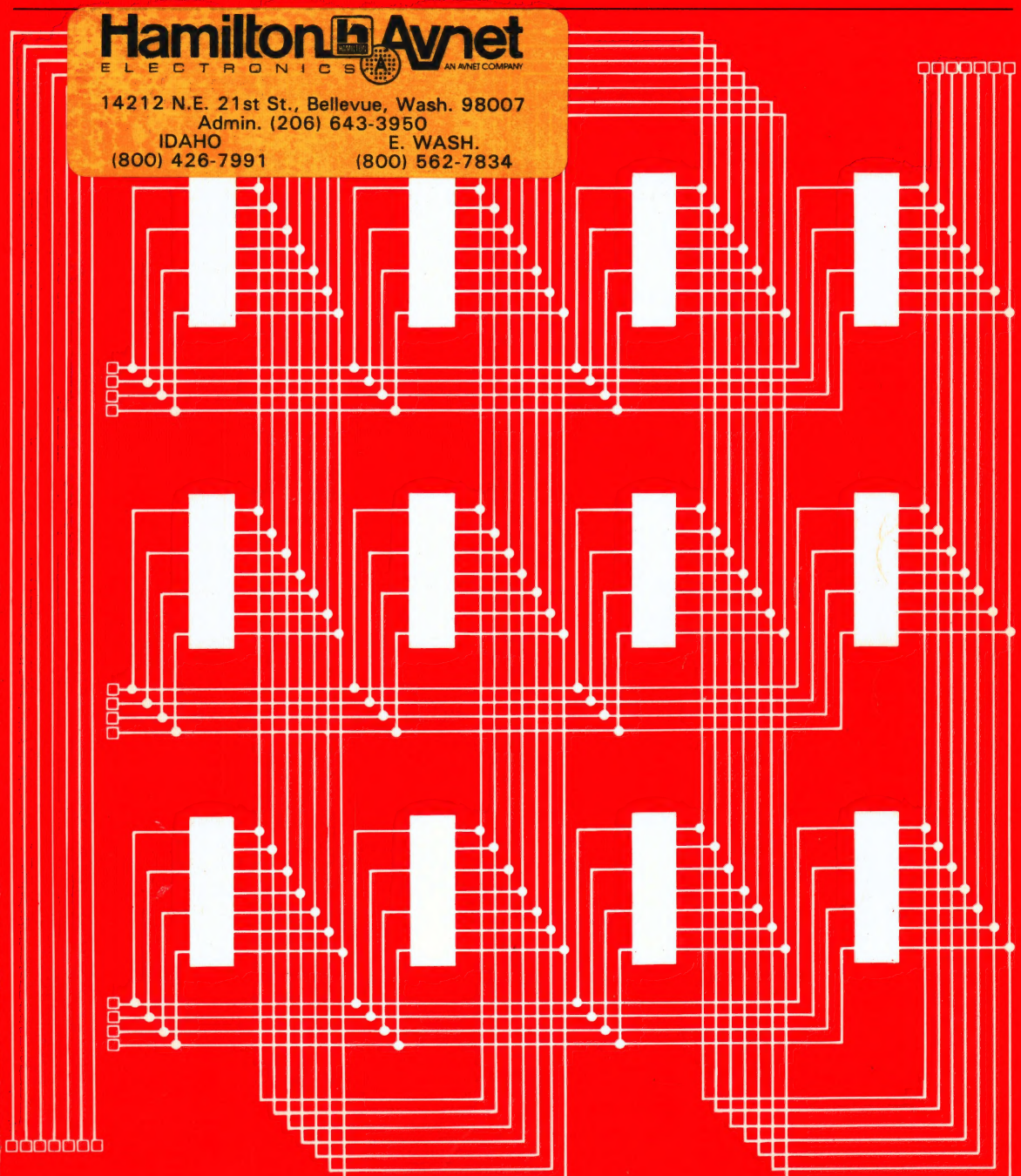
FAIRCHILD

A Schlumberger Company

Memory Data Book

1986



Handling Precautions for Semiconductor Components

The following handling precautions should be observed for oxide isolation, shallow junction processed parts, such as F100K ECL.

1. All Fairchild devices are shipped in conducting foam or antistatic tubes. When they are removed for inspection or assembly, proper precautions should be used.

2. Fairchild devices, after removal from their shipping material, should be placed leads down on a grounded surface. Under no circumstances should they be placed in polystyrene foam or non-conducting plastic trays used for shipment and handling of conventional ICs.

3. Individuals and tools should be grounded before coming in contact with these devices.

4. Do not insert or remove devices in sockets with power applied. Ensure that power supply transients, such as occur during power turn-on or off, do not exceed maximum ratings.

5. In the system, all unused inputs must be connected to either a logic HIGH or logic LOW level such as V_{EE} or the output of a logic element.

6. After assembly on PC boards, ensure that static discharge cannot occur during handling, storage or maintenance. Boards may be stored with their connectors surrounded with conductive foam.

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Memory Data Book

$4.95

Memory and High Speed Logic

Memory and High Speed Logic
P.O. Box 5000 M/S 2C17
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206/841-6000 TWX 510 101 0846

Table of Contents

Numerical Index of Devices

Numerical Index of Devices (Cont'd)

Selection Guide

TTL PROMs

TTL Programmable Logic

ECL/TTL/CMOS RAMs and PROMs Cross Reference Guide

FSC P/N	Org	Output	T_{AA}	Pkg Pins	Other Features	AMD	Harris	Hitachi	INMOS
10145A	16x4	ECL	9	24	REG FILE			HD10145	
100145	16x4	ECL	9	24	REG FILE			HD100145	
10402	16x4	ECL	6	16	REG FILE				
100402	16x4	ECL	6	16	REG FILE				
10415	1Kx1	ECL	10	16		AM10415		HM2110/12	
100415	1Kx1	ECL	10	16		AM100415		HD100415	
10422	256x4	ECL	10	24		AM10422		HD10422	
100422	256x4	ECL	10	24		AM100422		HD100422	
93415	1Kx1	OC	30/25	16		AM93415			
93L415	1Kx1	OC	45/35	16					
93425	1Kx1	TS	30/25	16		AM93425			
93L425	1Kx1	TS	45/35	16					
93419	64x9	OC	45/35	28					
93422	256x4	TS	45/35	22		AM93422			
93L422	256x4	TS	60/45	22		AM93L422			
93479	256x9	TS	45/35	22					
10Z416	256x4	ECL	20	16					
100Z416	256x4	ECL	20	16					
93Z450	1Kx8	OC	40/35	24		AM27S180	HM7680	HN25088	
93Z450	1Kx8	OC	40/35	24	SLIMLINE	AM27S280			
93Z451	1Kx8	TS	40/35	24		AM27S181	HM7681	HN25089	
93Z451	1Kx8	TS	40/35	24	SLIMLINE	AM27S281			
93Z510	2Kx8	OC	45	24		AM27S190		HN25168	
93Z510	2Kx8	OC	45	24	SLIMLINE	AM27S290			
93Z511	2Kx8	TS	45	24		AM27S191	HM76161	HN25169	
93Z511	2Kx8	TS	45	24	SLIMLINE	AM27S291			
93Z564	8Kx8	OC	55/45	24					
93Z565	8Kx8	TS	55/45	24		AM27S49	HM76641		
F1600	64Kx1	SMOS	70/55/45	22				HN6287	IMS1600

Fujitsu	MMI	Motorola	Nat'l	NEC	Raytheon	Signetics	TI
		MCM10145				10145	
		MCM10H145					
MBM10415			DM10415			10415	
MBM100415						100415	
MBM10422			DM10422			10422	
MBM100422						100422	
		MCM93415					
		MCM93425					
		MCM93422					
		MCM93L422					
						S82S212	
		MCM10149				10149	
						100149	
MB7131	53/6380	MCM7680	DM87S180	uBP409	29630	N82S180	TBP28SA86
MB7131SK			DM87S280				TBP28S86
MB7132	53/6381	MCM7681	DM87S181	uBP417	29631	N82S181	TBP28S86
MB7132SK			DM87S281				TBP28S86
MB7137		MCM76160	DM87S190	uBP409	29680	N82S190	TBP28SA166
MB7137SK			DM87S290			N82S190	TBP28S166
MB7138	63S1681	MCM76161	DM87S191	uBP429	29681	N82S191	
MB7138SK			DM87S291			N82S191	
MB7143							
MB7144							
				uBP4361			

Fairchild Memory Products Listed on Military Jan Qualified Products List (QPL) — 38510[3]

Jan Part Numbering System

J	M38510/	231	02	B	E	B
Jan Designator Cannot be Marked "J" Unless Qualified by DESC-EQM	General Procurement Spec	Refers to Slash Sheet	Defines Device Type	Processing Level S B	Defines Package Type Per Slash Sheet	Lead Finish A Hot Solder Dip B Tin Plate C Gold Plate X Lead Finish A,B, or C

TTL RAMs

Fairchild Generic P/N[1]	Jan Slash No.[2]	Jan QPL Part	Organization	Access Time (T_{AA})
93422DMQB	23110BWA	II	256X4, TS	60 ns
FMQB	23110BXA	II	256X4, TS	60 ns
LMQB	23110BYC	II	256X4, TS	60 ns
93422ADMQB	23114BWA	II	256X4, TS	45 ns
AFMQB	23114BXA	II	256X4, TS	45 ns
ALMQB	23114BYC	II	256X4, TS	45 ns
93L422DMQB	23112BWA	I	256X4, TS, LP	75 ns
FMQB	23112BXA	I	256X4, TS, LP	75 ns
LMQB	23112BYC	I	256X4, TS, LP	75 ns
93L422ADMQB	23115BWA	I	256X4, TS, LP	55 ns
AFMQB	23115BXA	I	256X4, TS, LP	55 ns
ALMQB	23115BYC	I	256X4, TS, LP	55 ns
93L415DMQB	23103BEA	I	1KX1, OC	70 ns
FMQB	23103BFA	I	1KX1, OC	70 ns
93425DMQB	23102BEA	I	1KX1, TS	60 ns (TWSA=15, TWHD=5)
	23106BEA	I	1KX1, TS	60 ns (TWSA=10, TWHD=10)
FMQB	23102BFA	I	1KX1, TS	60 ns (TWSA=15, TWHD=5)
	23106BFA	I	1KX1, TS	60 ns (TWSA=10, TWHD=10)
93425ADMQB	23108BEA	I	1KX1, TS	45 ns
FMQB	23108BFA	I	1KX1, TS	45 ns
93L425DMQB	23104BEA	I	1KX1, TS, LP	70 ns
FMQB	23104BFA	I	1KX1, TS, LP	70 ns
93L425ADMQB	23113BEA	I	1KX1, TS, LP	50 ns
FMQB	23113BFA	I	1KX1, TS, LP	50 ns

TTL PROMs

Fairchild Generic P/N[1]	Jan Slash No.[2]	Jan QPL Part	Organization	Access Time (T_{AA})
93Z511DMQB	21002BJA	I	2KX8, TS	100 ns
	21004BJA	I	2KX8, TS	55 ns

Notes

[1]Fairchild HI-REL generic QB product is processed to Hi-Rel level QB flow (in full compliance with MIL-STD-883) of Figure 2-2 and tested to the limits specified in individual data sheets under DC, AC, and functional (FN) performance characteristics.

[2]Fairchild JAN product is processed to HI-REL JAN flow per MIL-M38510 and MIL-STD-883 and tested per the DC, AC, and FN performance characteristics of the respective military slash sheet.

[3]Check Qualified Product List (QPL) — 38510 for current JAN listings.

Legend

TS = Three-State
A = Highspeed Version
OC = Open Collector
LP = Low Power Version

Notes

Quality Assurance and Reliability

Introduction
All Fairchild Memory and High Speed Logic Products are manufactured to strict quality and reliability standards. Product conformance to these standards is insured by careful monitoring of the following functions: (1) incoming quality inspection, (2) process quality control, (3) quality assurance, and (4) reliability.

Incoming Quality Inspection
Purchased piece parts and raw materials must conform to purchase specifications. Major monitoring programs are the inspection of package piece parts, inspection of raw silicon wafers, and inspection of bulk chemicals and materials. Two other important functions of incoming quality inspection are to provide real-time feedback to vendors and in-house engineering, and to define and initiate quality improvement programs.

Package Piece Parts Inspection
Each shipment of package piece parts is inspected and accepted or rejected based on AQL sampling plans. Inspection tests include both inherent characteristics and functional use tests. Inherent characteristics include physical dimensions, color, plating quality, material purity, and material density. Functional use tests for various package piece parts include die attach, bond pull, seal, lid torque, salt atmosphere, lead fatigue, solderability, and mechanical strength. In these tests, the piece parts are sent through process steps that simulate package assembly. The units are then destructively tested to determine whether or not they meet the required quality and reliability levels.

Silicon Wafer Inspection
Each shipment of raw silicon wafers is accepted or rejected based on AQL sampling plans. Raw silicon wafers are subjected to non-destructive and destructive tests. Included in the testing are flatness, physical dimensions, resistivity, oxygen and carbon content, and defect densities. The test results are used to accept or reject the lot.

Bulk Chemical and material Inspection
Bulk chemicals and materials play an important role in any semiconductor process. To insure that the bulk chemicals and materials used in processing Fairchild wafers are the highest quality, they are stringently tested for trace impurities and particulate or organic contamination. Mixtures are also analyzed to verify their chemical make-up.

Incoming inspection is only the first step in determining the acceptability of bulk chemicals and materials. After acceptance, detailed documentation is maintained to correlate process results to various vendors and to any variations found in mixture consistency.

Process Quality Control
Process quality is maintained by establishing and maintaining effective controls for monitoring the wafer fabrication process, reporting the results of the monitors, and initiating valid measurement techniques for improving quality and reliability levels.

Methods of Control
The process quality control program utilizes the following methods of control: (1) process audits, (2) environmental monitors, (3) process monitors, (4) lot acceptance inspections, (5) process qualifications, and (6) process integrity audits. These methods of control, defined below, characterize visually and electrically the wafer fabrication operation.

Process Audit — Audits concerning manufacturing operator conformance to specification. These are performed on all operations critical to product quality and reliability.

Environmental Monitor-Monitors concerning the process environment, *i.e.*, water purity, air temperature/humidity, and particulate count.

Process Monitor — Periodic inspection at designated process steps for verification of manufacturing inspection and maintenance of process average. These inspections provide both attribute and variables data.

Lot Acceptance — Lot by lot sampling. This sampling method is reserved for those operations deemed as critical and, as such, requiring special attention.

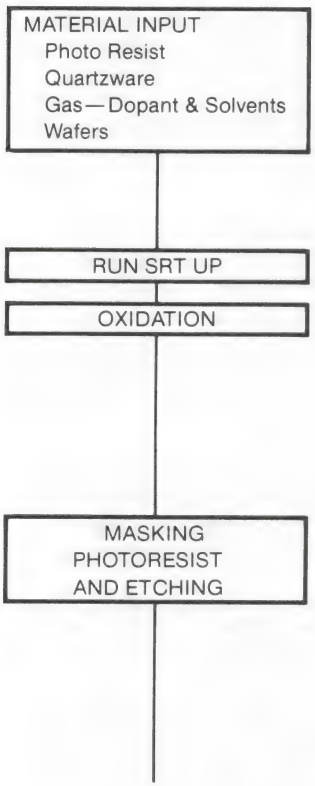
Process Qualification — Complete distributional analysis is run to specified tolerance averages and standard deviations. These qualifications are typically conducted on deposition and evaporation processes, *i.e.*, epi, aluminum, vapox, and backside gold.

Process Integrity Audit — Special audits conducted on oxidation and metal evaporation processes (CV drift—oxidation; SEM evaluation — metal evaporation).

Data Reporting
Process quality control data is recorded on an attribute or variable basis as required; control charts are maintained on a regular basis. This data is reviewed at periodic intervals and serves as the basis for judging the acceptability of specific processes. Summary data from the various process quality control operations are relayed to cognizant line, engineering and management personnel in real time so that, if appropriate, the necessary corrective actions can be immediately taken.

Process Flow
Figure 2-1 shows the integration of the various methods of control into the wafer fabrication process flow. The process flow chart contains examples of the process quality controls and inspections utilized in the manufacturing operation.

Fig. 2-1 Process Flow Chart



Process Controls (Examples)

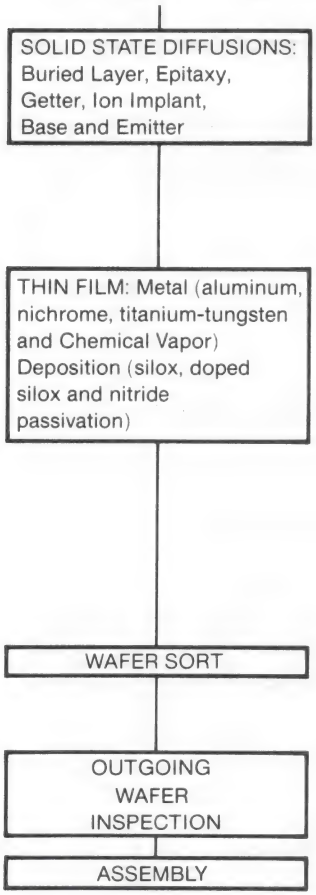
A. Environmental
B. Chemical supplies
C. Substrate exam. (resistivity, flatness, thickness, crystal perfection, etc.)
D. Photoresist evaluation
E. Mask inspections

A. Process audit

A. Process audit/qualification
B. Environmental
C. Process monitors (thickness, pinhole and crack measurements)
E. C V Plotting
F. Calibration

A. Process audits
B. Environmental
C. Visual examinations
D. Photoresist evaluation (preparation, storage, application, baking, development and removal),
E. Etchant controls
F. Exposure controls (intensity, uniformity)

Fig. 2-1 Process Flow Chart (cont'd.)



A. Process audits/qualification
B. Environmental
C. Temperature profiling
D. Quartz cleaning
E. Calibration
F. Electrical tests (resistivity, breakdown voltages, etc.)

A. Process audits/qualification
B. Environmental
C. Visual examinations
D. Epitaxy controls (thickness, resistivity cleaning, visual examination)
E. Metallization controls (thickness, temperature cleaning, SEM, C V plotting)
F. Glassivation controls (thickness, dopant concentraton, pinhole and crack measurements)

A. Process audit
B. Environments
C. Visual examinations

A. Process audit
B. Inspection

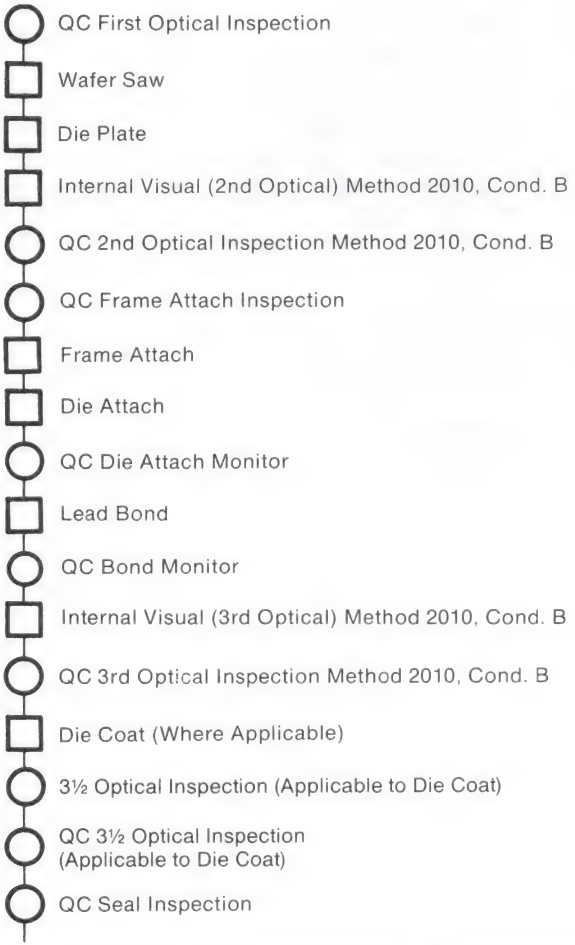
Quality Assurance

To assure that all product shipped meets both internal Fairchild specifications for standard product and customer specifications in the case of negotiated specs, a number of QA inspections throughout the assembly process flow (*Figure 2-2*) are required.

The Hi-Rel and Standard Rel Assembly and Test Flows are shown below to provide a clearer understanding of the operations performed. Flows, much more detailed than the flows in Figures 2-2 and 2-3, govern the assembly and test of devices to Fairchild's specifications.

The Product built to the Hi-Rel Level B Assembly and Test Flow meet the requirements of MIL-STD-883 (Test Methods and Procedures for Microcircuits).

Fig. 2-2 HI-REL (Level B) Assembly and Test Flow (per MIL-STD-883, Methods 5004, 5005)



QC PDA Verification

QC Group A Electrical Test (Room)

Electrical Test (Cold)

QC Group A Electrical Test (Cold)

Solder Finish (Where Applicable)

QC Solder Lead Finish Inspection (Where Applicable)

Fine Leak (DIP's & LCC's) Method 1014, Cond. B

Gross Leak (DIP's & LCC's) Method 1041, Cond. C

Mark

Electrical Test (Hot)

QC Group A, Electrical Test (Hot)

Programmability Sample (When Applicable)

Electrical Test (Hot) of Programmed Samples (When Applicable)

Electrical Test (Cold) of Programmed Samples (When Applicable)

Electrical Test (Room) of Programmed Samples (When Applicable)

External Visual Inspection, Method 2009

QC External Visual Inspection

QC Fine & Gross Leak Methods 1014, Cond. B & Method 1014, Cond. C (Subgroup B-7)

DC Electrical Screen of QC Seal Test Samples

External Visual of QC Seal Test Samples, Method 2009

QC Internal Visual/Mechanical Method 2014 (Subgroup B-4)

QC Solderability Method 2003 (Subgroup B-3)

QC Bond Strength Method 2011 (Subgroup B-5)

QC Resistance to Solvents Methods 2015 (Subgroup B-2)

QC Physical Dimensions Method 2016 (Subgroup B-1)

Pack

Quality Conformance Inspection (QCI) Method 5005 (Group C & D)

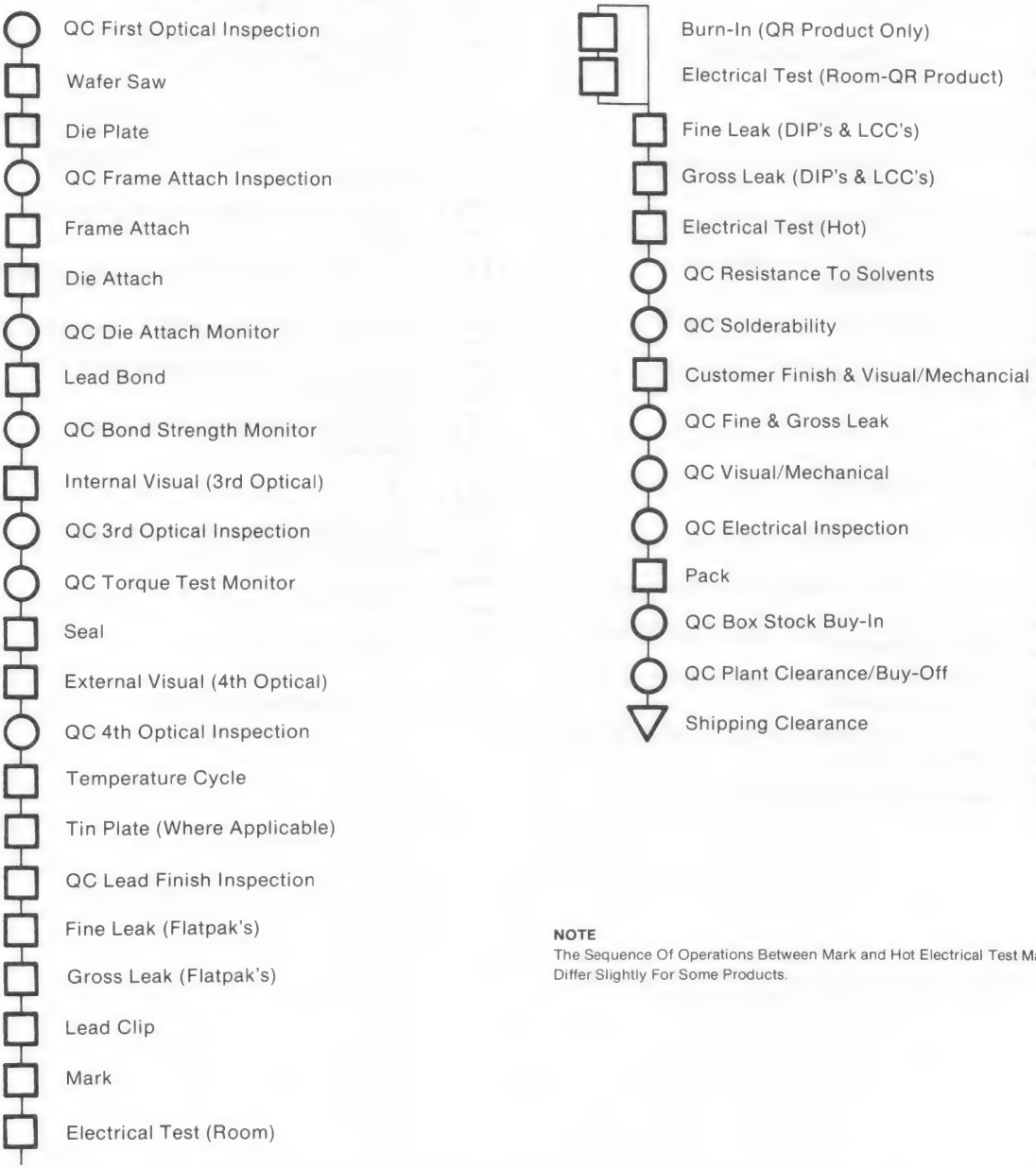
QC Data Check

Shipping Clearance

QA Plant Clearance/Buy-Off

NOTE
The sequence of Operations Between Pre Burn-in Electrical Test and Hot Electrical Test May Differ Slightly for some products.

Fig. 2-3 STD-REL Assembly and Test Flow



NOTE
The Sequence Of Operations Between Mark and Hot Electrical Test May Differ Slightly For Some Products.

Reliability

A number of programs, among them qualification testing, reliability monitoring, failure analysis, and reliability data collection and presentation, are maintained.

Qualification Programs

All products receive reliability qualification prior to the product being released for shipment. Qualification is required for (1) new product designs, (2) new fabrication processes or (3) new packages or assembly processes. Stress tests are run in accordance to test methods described in MIL-STD-883. Test results are evaluated against existing reliability levels, and must be better than or equal to current product for the new product to receive qualification.

New Product Designs — Receive, as a minimum, +125° C operating life tests. Readouts are normally scheduled at 168 hours, 500 hours, 1000 hours and 2000 hours. The samples stressed are electrically good units from initial wafer runs. Additional life testing, consisting of high-temperature operating life test, 85/85 humidity bias tests, bias pressure pot (BPTH) tests, mechanical series or thermal series may be run as deemed necessary. Redesigns of existing device layouts are considered to be new product designs, and full qualification is necessary.

New Fabrication Processes — Qualifications are designed to evaluate the new process against the current process. Stress tests consist of operating life test, high-temperature operating life test, 85/85 humidity bias test and/or biased pressure pot (BPTH) test. In addition, package environment tests may be performed, such as Thermal Series or Mechanical Series. Evaluations are performed on various products throughout the development stages of the new process. Units stressed are generally from split wafer runs. All processing is performed as a single wafer lot up to the new process steps, where the lot is split for the new and the current process steps. Then the wafers are recombined, and again processed as a single wafer lot. This allows for controlled evaluation of the new process against the standard process. Both significant modifications to existing process and transferring existing products to new fabrication plants are treated as a new process.

New Packages or Assembly Processes — Qualifications are performed for new package designs, changes to existing piece parts, changes in piece part vendors, and significant modification to assembly process methods. In general, samples from three assembly runs are stressed to a matrix in accordance to MIL-STD-883, Method 5005, group B, group C, subgroup 2, and group D (*Table 2-1*). In addition, +100°C operating life tests, 85/85 humidity bias tests, biased pressure pot (BPTH) tests and unbiased pressure pot tests are performed for plastic packages.

Reliability Monitors

Reliability testing of mature products is performed to establish device failure rates, and to identify problems occuring in production. Samples are obtained on a regular basis from production. These units are stressed with operating life tests or package environmental tests. The results of these tests are summarized and reported. When a problem is identified, the respective engineering group is notified, impact on the customer is reviewed and a corrective action plan is implemented.

Current testing levels are in excess of 14,000 units per year stressed with operating life tests, and 23,000 units per year stressed with package environmental tests.

Failure Analysis

Failure analysis is performed on all units failing reliability stress tests. Failure analysis is offered as a service to support manufacturing and engineering, and to support customer returns and customer requested failure studies. The failure analysis procedure used has been established to provide a technique of sequential analysis. This technique is based on the premise that each step of analysis will provide information of the failure without destroying information to be obtained from subsequent steps. The ultimate purpose is to uncover all underlying failure mechanisms through complete, in-depth, defect analysis. The procedure places great emphasis on electrical analysis, both external before decapsulation, and internal micro-probing. Visual examinations with high magnification microscopes or SEM analysis are used to confirm failure mechanisms. Results of the failure analysis are recorded and, if abnormalities are found, reported to engineering and/or manufacturing for corrective action.

Data Collection and Presentation

Product reliability is controlled by first stressing the product, and then feeding back results to manufacturing and engineering. This feedback takes two forms. There

is a formal monthly Reliability Summary distributed to all groups. The summary shows current product failure rates, highlights problem areas, and shows the status of qualification and corrective action programs. Less formal feedback is obtained by including reliability personnel at all product meetings, which gives high visibility to the reliability aspects of various products. As a customer service, product reliability data is compiled and made available upon request.

Table 2-1 Package Environmental Stress Matrix

Test	MIL-STD-883	
	Method	**Condition**
Group B		
Subgroup 1		
Physical dimensions	2016	
Subgroup 2		
Resistance to solvents	2015	
Subgroup 3		
Solderability	2003	Soldering temperature $+245 \pm 5°C$, $+260 \pm 5°C$ (L_{CC} only)
Subgroup 5		
Bond strength	2011	
(1) Thermocompression		(1) Test condition C or D
(2) Ultrasonic or wedge		(2) Test condition C or D
Group C		
Subgroup 2		
Temperature cycling	1010	Test condition C ($-65°C$ to $+150°C$)
Constant acceleration	2001	Test condition E (30Kg), Y_1 orientation and X_1 orientation (where available) Test condition D (20K g) for packages over 5 gram weight or with seal ring greater than 2 inches
Seal	1014	
(a) Fine		
(b) Gross		
Visual examination		
End-point electrical parameters		
Group D		
Subgroup 2		
Lead integrity	2004	Test condition B2 (lead fatigue)
Seal	1014	As applicable
(a) Fine		
(b) Gross		

Table 2-1 Package Environmental Stress Matrix (cont'd.)

Test	MIL-STD-883 Method	MIL-STD-883 Condition
Subgroup 3		
Thermal shock	1011	Test condition B (-55°C to +125°C) 15 cycles minimum
Temperature cycling	1010	Test condition C (-65°C to +150°C) 100 cycles minimum
Moisture resistance	1004	
Seal	1014	
(a) Fine		
(b) Gross		
Visual examination		
End-point electrical parameters		
Subgroup 4		
Mechanical shock	2002	Test condition B (1500G, 0.5 ms)
Vibration, variable frequency	2007	Test condition A (20G)
Constant acceleration	2001	Same as group C, subgroup 2
Seal	1014	
(a) Fine		
(b) Gross		
Visual examination		
End-point electrical parameters		
Subgroup 5		
Salt atmosphere	1009	Test condition A minimum (24 hours)
Seal	1014	As applicable
(a) Fine		
(b) Gross		
Visual examination		
Subgroup 6		
Internal water-vapor content	1018	
Subgroup 7		
Adhesion of lead finish	2025	
Subgroup 8		
Lid Torque	2024	As applicable (prior to 883C, this test was part of Subgroup D-7)
Other tests performed which are not included in Group B, C or D:		
Die Shear	2019	
Radiography	2012	(Prior to 1984, this test was not performed)

Notes

F100K DC Family Specifications

DC characteristics for the F100K series family parametric limits listed below are guaranteed for the entire F100K ECL family unless specified on the individual data sheet.

Absolute Maximum Ratings: Above which the useful life may be impaired[1]

Storage Temperature	−65° C to +150° C
Maximum Junction Temperature (T_J)	+175° C
Supply Voltage Range	−7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	−50 mA
Operating Range[2]	−5.7 V to −4.2 V
Lead Temperature (Soldering 10 sec)	300° C

DC Characteristics: V_{EE} = −4.5 V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, Note 3

Symbol	Characteristic	Min	Max	Unit	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−880	mV	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	Loading with 50 Ω to −2.0 V
V_{OL}	Output LOW Voltage	−1810	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035		mv	V_{IN} = $V_{IH(min)}$ or $V_{IL(max)}$	
V_{OLC}	Output LOW Voltage		−1610	mV		
V_{IH}	Input HIGH Voltage	−1165	−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		μA	V_{IN} = $V_{IL(min)}$	

1. Unless specified otherwise on individual data sheet.
2. Parametric values specfied at −4.8 V to −4.2 V.
3. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

All ECL RAM products (except for Register File RAMs) in ceramic packages: dual-in-line, and flatpak are polyimide die-coated to decrease sensitivity to alpha particles emitted primarily by the seal glass and ceramic of the package.

DC Characteristics: $V_{EE} = -4.2$ V, $V_{CC} = V_{CCA} = GND$, $T_C = 0°C$ to $+85°C$, Note 3

Symbol	Characteristic	Min	Max	Unit	Conditions	
V_{OH}	Output HIGH Voltage	−1020	−870	mV	$V_{IN} = V_{IH(max)}$ or $V_{IL(min)}$	Loading with 50 Ω to −2.0 V
V_{OL}	Output LOW Voltage	−1810	−1605	mV		
V_{OHC}	Output HIGH Voltage	−1030		mv	$V_{IN} = V_{IH(min)}$ or $V_{IL(max)}$	
V_{OLC}	Output LOW Voltage		−1595	mV		
V_{IH}	Input HIGH Voltage	−1150	−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		μA	$V_{IN} = V_{IL(min)}$	

DC Characteristics: $V_{EE} = -4.8$ V, $V_{CC} = V_{CCA} = GND$, $T_C = 0°C$ to $+85°C$, Note 3

Symbol	Characteristic	Min	Max	Unit	Conditions	
V_{OH}	Output HIGH Voltage	−1035	−880	mV	$V_{IN} = V_{IH(max)}$ or $V_{IL(min)}$	Loading with 50 Ω to −2.0 V
V_{OL}	Output LOW Voltage	−1830	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1045		mv	$V_{IN} = V_{IH(min)}$ or $V_{IL(max)}$	
V_{OLC}	Output LOW Voltage		−1610	mV		
V_{IH}	Input HIGH Voltage	−1165	−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810	−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		μA	$V_{IN} = V_{IL(min)}$	

Notes on preceding page

F10K DC Family Specifications

DC characteristics for the F10K series memories. Parametric limits listed below are guaranteed for all F10K memories, except where noted on individual data sheets.

Absolute Maximum Ratings: Above which the useful life may be impaired[2]

Storage Temperature	−65° C to +150° C
Maximum Junction Temperature (T_J)	+175° C
V_{EE} Pin Potential to Ground Pin	−7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	−30 mA to +0.1 mA
Lead Temperature (Soldering 10 sec)	300° C

Guaranteed Operating Ranges

Supply Voltage (V_{EE})			Case Temperature (T_C)
Min	Typ	Max	
−5.46 V	−5.2 V	−4.94 V	0°C to +75°C

DC Characteristics: V_{EE} = -5.2 V, $V_{CC} = V_{CCA}$ = GND, T_C = 0° C to + 75° C[1]

Symbol	Characteristic	Min	Max	Unit	T_C	Conditions[2]	
V_{OH}	Output HIGH Voltage	−1000 −960 −900	−840 −810 −720	mV	0°C +25°C +75°C	$V_{IN} = V_{IH(max)}$ or $V_{IL(min)}$	Loading is 50 Ω to −2.0 V
V_{OL}	Output LOW Voltage	−1870 −1850 −1830	−1665 −1650 −1625	mV	0°C +25°C +75°C		
V_{OHC}	Output HIGH Voltage	−1020 −980 −920		mv	0°C +25°C +75°C	$V_{IN} = V_{IH(min)}$ or $V_{IL(max)}$	
V_{OLC}	Output LOW Voltage		−1645 −1630 −1605	mV	0°C +25°C +75°C		
V_{IH}	Input HIGH Voltage	−1145 −1105 −1045	−840 −810 −720	mV	0°C +25°C +75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input LOW Voltage	−1870 −1850 −1830	−1490 −1475 −1450	mV	0°C +25°C +75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IL}	Input LOW Current	0.5	170	μA	+25°C	$V_{IN} = V_{IL(min)}$	

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Unless specified otherwise on individual data sheet.

FAIRCHILD
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F100145
16 x 4-Bit Register File (RAM)

Memory and High Speed Logic

Description

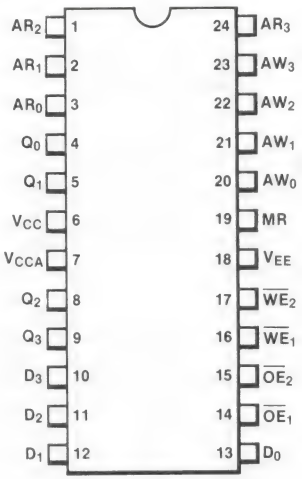
The F100145 is a 64-bit register file organized as 16 words of four bits each. Separate address inputs for Read (AR_n) and Write (AW_n) operations reduce overall cycle time by allowing one address to be setting up while the other is being executed. Operating speed is also enhanced by four output latches which store data from the previous read operation while writing is in progress. When both Write Enable ($\overline{WE}$) inputs are LOW, the circuit is in the Write mode and the latches are in a Hold mode. When either $\overline{WE}$ input is HIGH, the circuit is in the Read mode, but the outputs can be forced LOW by a HIGH signal on either of the Output Enable ($\overline{OE}$) inputs. This makes it possible to tie one $\overline{WE}$ input and one $\overline{OE}$ input together to serve as an active-LOW Chip Select ($\overline{CS}$) input. When this wired $\overline{CS}$ input is HIGH, reading will still take place internally and the resulting data will enter the latches and become available as soon as the $\overline{CS}$ signal goes LOW, provided that the other $\overline{OE}$ input is LOW. A HIGH signal on the Master Reset (MR) input overrides all other inputs, clears all cells in the memory, resets the output latches, and forces the outputs LOW.

Pin Names

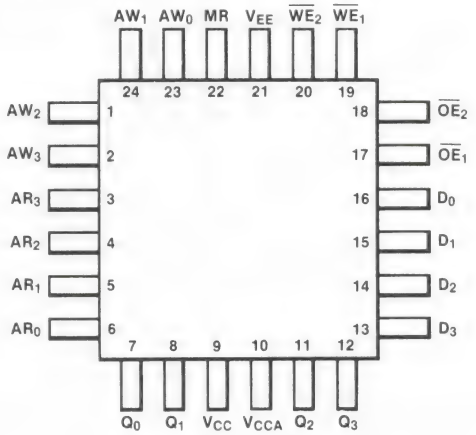
AR_0–AR_3	Read Address Inputs
AW_0–AW_3	Write Address Inputs
$\overline{WE}_1$, $\overline{WE}_2$	Read Enable Inputs (Active LOW)
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Inputs (Active LOW)
D_0–D_3	Data Inputs
MR	Master Reset Input
Q_0–Q_3	Data Outputs

Connection Diagrams

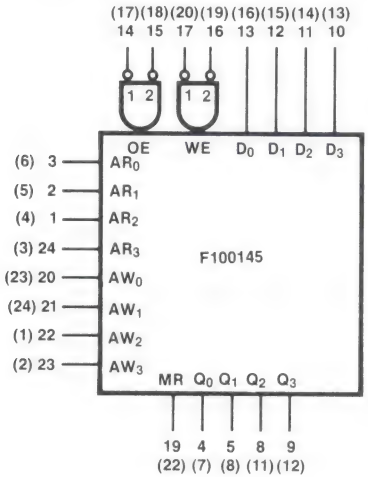
24-Pin DIP (Top View)



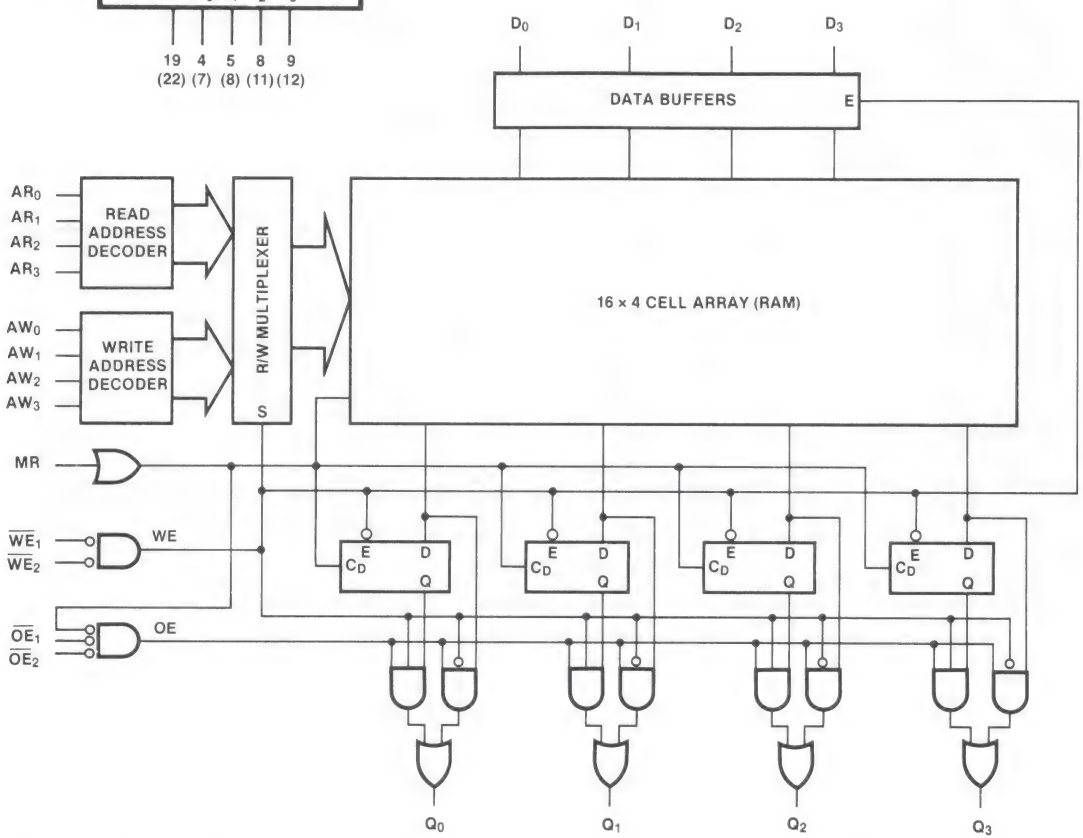
24-Pin Flatpak (Top View)



Logic Symbol and Logic Diagram



V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many internal functions are achieved more efficiently than indicated.

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current All Inputs			240	μA	$V_{IN} = V_{IH(max)}$
I_{EE}	Power Supply Current	−247	−170		mA	Inputs Open

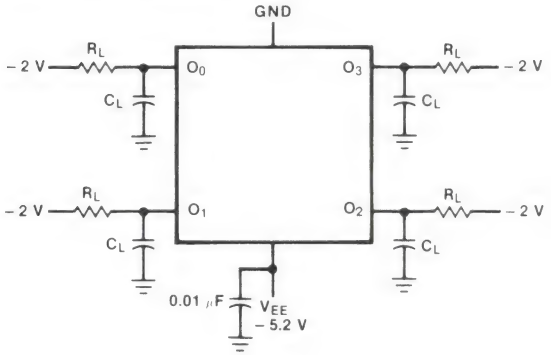
*See Family Characteristics for other dc specifications.

AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
	Access/Recovery Timing								
t_{AA}	Address Access[1]	2.20	7.40	2.20	7.40	2.20	7.60	ns	*Figures 1* and *3a*
t_{OR}	Output Recovery	1.00	2.90	1.10	2.90	1.10	3.20	ns	*Figures 1* and *3e*
t_{OD}	Output Disable	1.00	2.90	1.10	2.90	1.10	3.20	ns	
	Read Timing								
t_{RSA1}	Address Setup	1.10		1.10		1.10		ns	*Figures 1* and *3b*
t_{WEQ}	Output Delay	2.00	5.00	2.00	5.00	2.00	5.50	ns	
	Output Latch Timing								
t_{RSA2}	Address Setup	4.10		4.10		5.60		ns	*Figures 1* and *3c*
t_{RHA}	Address Hold	0.10		0.10		0.10		ns	*Figures 1* and *3d*
	Write Timing								
t_{WSA}	Address Setup	0.10		0.10		0.10		ns	
t_{WHA}	Address Hold	1.10		1.60		1.60		ns	
t_{WSD}	Data Setup	1.10		1.60		1.90		ns	t_W = 6.0 ns
t_{WHD}	Data Hold	1.10		1.60		1.90		ns	*Figures 1* and *4*
t_W	Write Pulse Width, LOW	4.60		5.00		5.50		ns	
	Master Reset Timing								
t_M	Reset Pulse Width, LOW	4.50		4.50		5.00		ns	*Figures 1* and *5a*
t_{MHW}	$\overline{WE}$ Hold to Write	6.30		7.10		10.50		ns	
t_{MQ}	Output Disable	2.80		2.80		3.20		ns	*Figures 1* and *5b*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	2.30	0.50	2.30	0.50	2.30	ns	

1. The maximum address access time is guaranteed to be the worst case bit in memory using a pseudo random testing pattern.

Fig. 1 AC Test Circuit



Notes
All Timing Measurements Referenced to 50% of Input Levels
C_L = 3 pF including Fixture and Stray Capacitance
R_L = 50 Ω to -2.0 V

Fig. 2 Input Levels

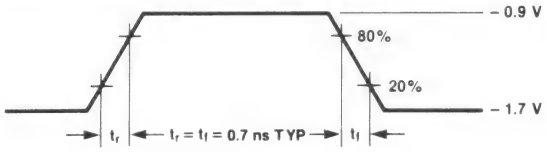
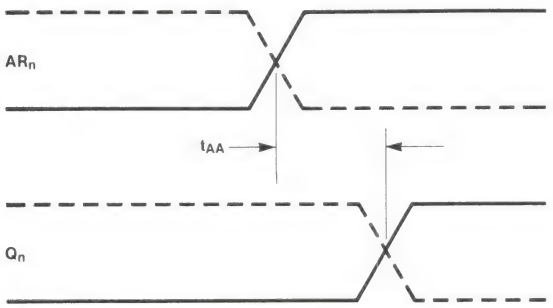
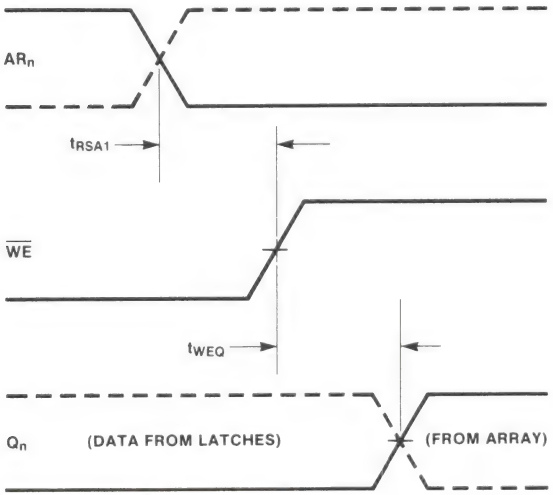


Fig. 3 Read Timing

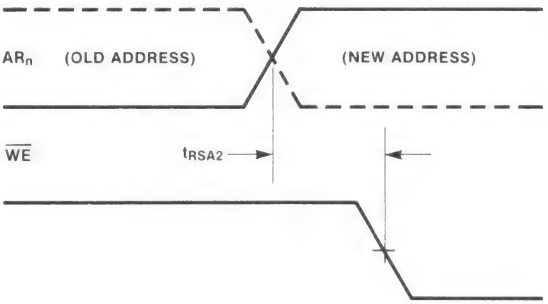
3a Address Access Time ($\overline{WE_1}$ or $\overline{WE_2}$ = HIGH; $\overline{OE_1}$ = $\overline{OE_2}$ = LOW)



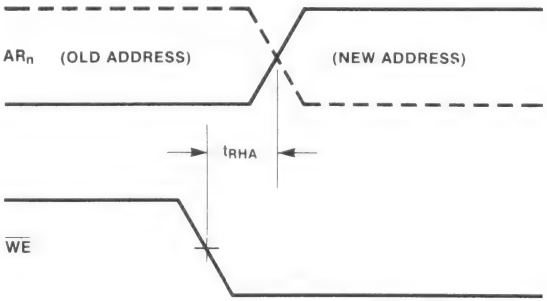
3b Address Setup Time before $\overline{WE}$, to Ensure Minimum Delay (unpulsed $\overline{WE}$= $\overline{OE_1}$ = $\overline{OE_2}$ = LOW)



3c Address Setup Time to Ensure Latching Data from New Address (unpulsed $\overline{WE}$ = LOW)



3d Address Hold Time to Ensure Latching Data from Old Address (unpulsed $\overline{WE}$ = LOW)



3e Output Recovery/Disable Times, $\overline{OE}$ to Qn (unpulsed $\overline{OE}$ = LOW)

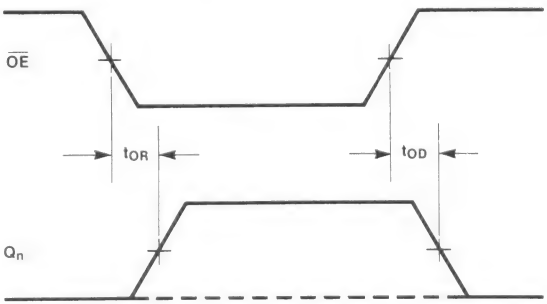


Fig. 4 Write Timing

Address and Data Setup and Hold Times;
Write pulse Width (unpulsed $\overline{WE}$ = LOW)

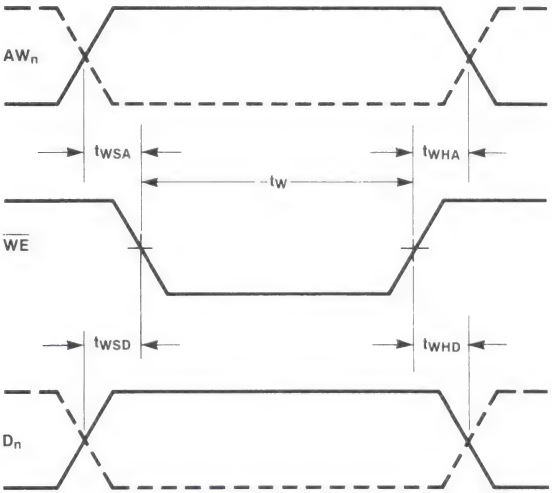
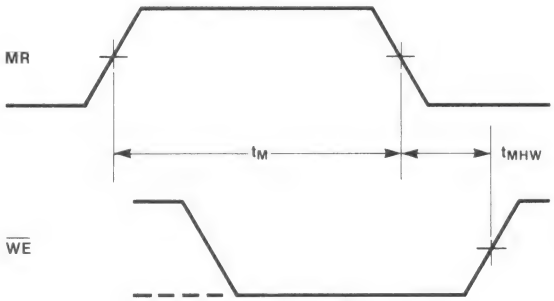
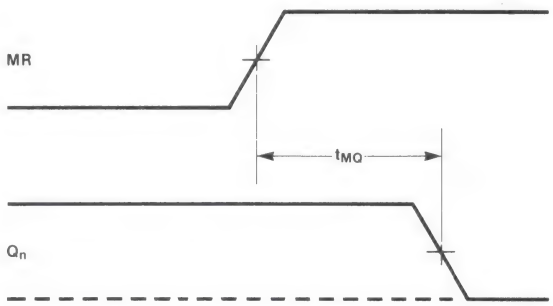


Fig 5 Master Reset Timing

5a Reset Pulse Width; $\overline{WE}$ Hold Time for Subsequent Writing (address already setup, unpulsed $\overline{WE}$ = LOW)

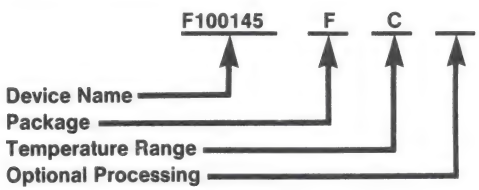


5b Output Reset Delay, MR to Q_n



3

Ordering Information



Packages and Outlines (See Section 9)
D = Ceramic DIP
F = Flatpak

Temperature Ranges
C = 0°C to +85°C. Case

Optional Processing
QR = 160 Hour Burn in

FAIRCHILD
A Schlumberger Company

F100402
16 x 4-Bit Register File (RAM)

Memory and High Speed Logic

Description

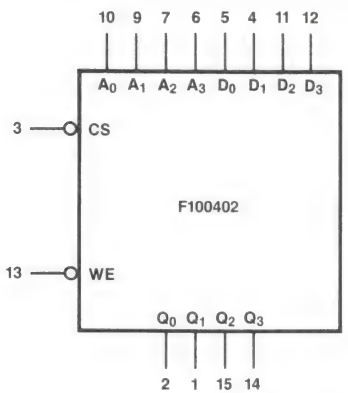
The F100402 is a high-speed 64-bit Random Access Memory (RAM) organized as a 16-word by 4-bit array. External logic requirements are minimized by internal address decoding, while memory expansion and data busing are facilitated by the output disabling features of the Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) inputs.

A HIGH signal on $\overline{CS}$ prevents read and write operations and forces the outputs to the LOW state. When $\overline{CS}$ is LOW, the $\overline{WE}$ input controls chip operations. A HIGH signal on $\overline{WE}$ disables the Data input (D_n) buffers and enables readout from the memory location determined by the Address (A_n) inputs. A LOW signal on $\overline{WE}$ forces the Q_n outputs LOW and allows data on the D_n inputs to be stored in the addressed location. Data exists in the same logical sense as presented at the data inputs, *i.e.*, the memory is non-inverting.

Pin Names

$\overline{CS}$	Chip Select Input
A_0–A_3	Address Inputs
D_0–D_3	Data Inputs
$\overline{WE}$	Write Enable Input
Q_0–Q_3	Data Outputs

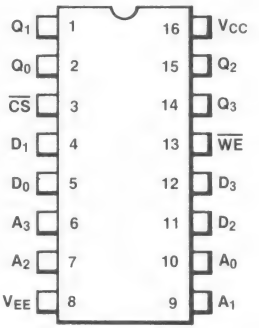
Logic Symbol



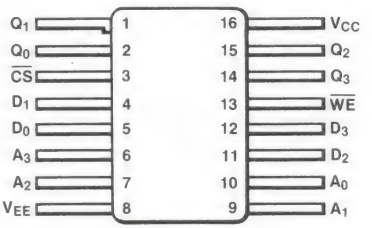
V_{CC} = Pin 16
V_{EE} = Pin 8

Connection Diagrams

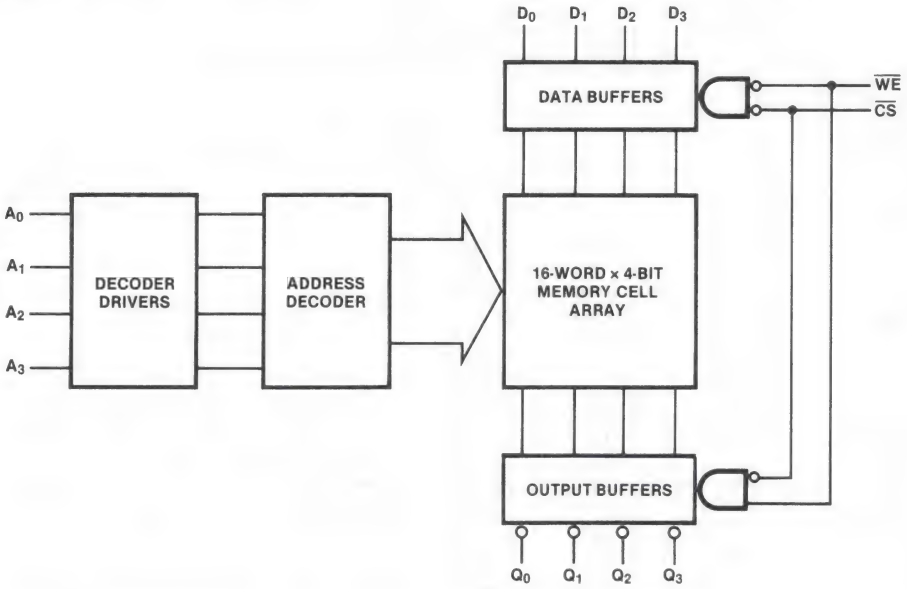
16-Pin DIP (Top View)



16-Pin Flatpak (Top View)



Logic Diagram



DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current All Inputs			300	μA	$V_{IN} = V_{IH(max)}$
I_{EE}	Power Supply Current	−170	−110		mA	Inputs Open

*See Family Characteristics for other dc specifications.

AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = GND, Applies to Flatpak and DIP Packages

Symbol	Characteristic	T_C = 0°C		T_C = +25°C		T_C = +85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
	Access/Recovery Timing								
t_{ACS}	Chip Select Access		3.30		3.50		3.80	ns	
t_{RCS}	Chip Select Recovery		3.30		3.50		3.80	ns	*Figures 1 and 4*
t_{AA}	Address Access[1]		5.00		5.30		6.00	ns	
	Write Timing, Setup								
t_{WSD}	Data	0.50		0.50		0.80		ns	
t_{WSCS}	Chip Select	1.50		1.50		1.50		ns	
t_{WSA}	Address	1.00		1.00		1.00		ns	*Figures 1 and 3*
	Write Timing, Hold								t_W = 6 ns
t_{WHD}	Data	0.50		0.50		0.50		ns	
t_{WHCS}	Chip Select	0.50		0.50		0.50		ns	
t_{WHA}	Address	2.50		2.50		2.50		ns	
t_{WR}	Write Recovery Time	4.00		4.00		4.50		ns	*Figures 1 and 4*
t_{WS}	Write Disable Time	3.00		3.00		3.50		ns	
t_W	Write Pulse Width, (LOW)	2.50		2.50		3.00		ns	*Figures 1 and 3*
t_{CS}	Chip Select Pulse Width, (LOW)	2.50		2.50		3.00		ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	1.70	0.50	1.70	0.50	1.70	ns	*Figures 1 and 4*

1. The maximum address access time is guaranteed to be the worst case bit in memory using a pseudo random testing pattern.

Fig. 1 AC Test Circuit

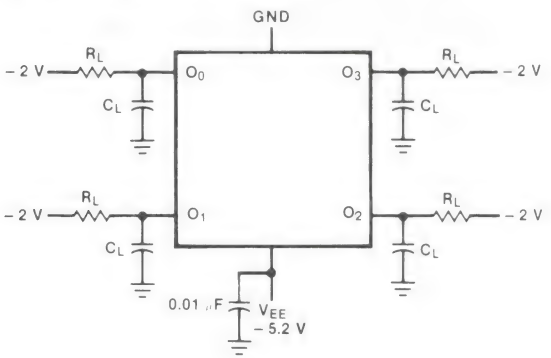
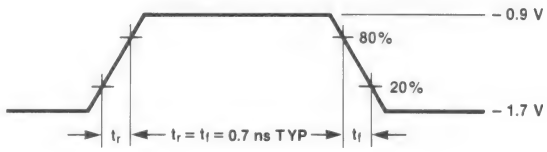


Fig. 2 Input Levels

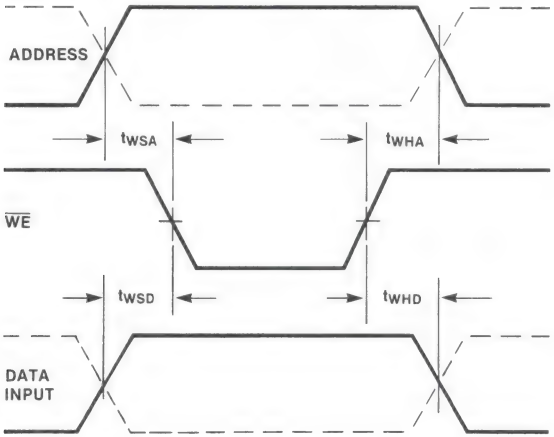


Notes
All Timing Measurements Referenced to 50% of Input Levels
C_L = 3 pF including Fixture and Stray Capacitance
R_L = 50 Ω to -2.0 V

Fig. 3 Write Modes

Write Enable Strobe

ADDRESS AND DATA INPUT SET-UP AND HOLD TIMES
(CS = LOW)



CHIP SELECT SET-UP AND HOLD TIMES

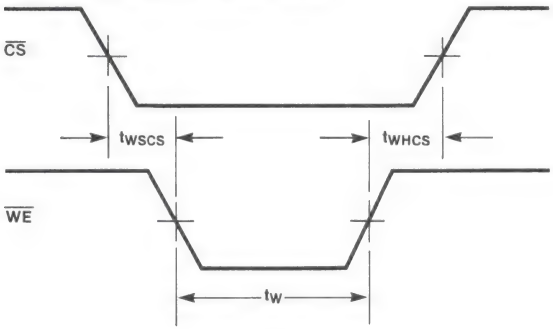
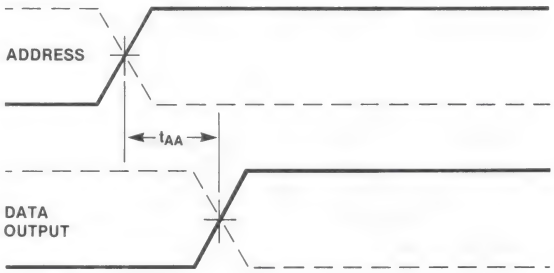


Fig. 4 Read Modes

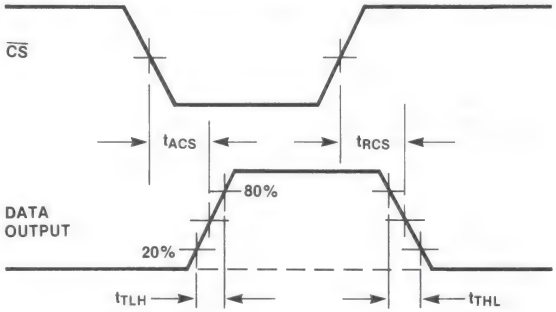
Address Input to Data Output (WE = HIGH, CS = LOW)

ADDRESS ACCESS TIME



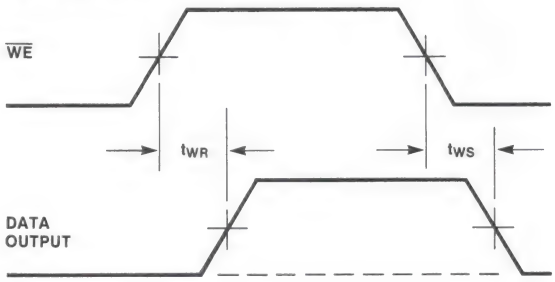
Chip Select Input to Data Output (WE = HIGH)

CHIP SELECT ACCESS AND RECOVERY TIMES

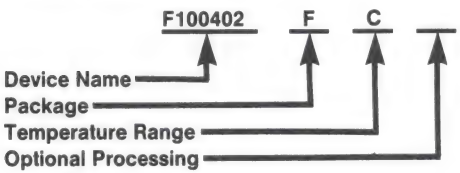


Write Enable Input to Data Output (CS = LOW)

WRITE RECOVERY, DISABLE TIMES



Ordering Information



Packages and Outlines (See Section 9)
D = Ceramic DIP
F = Flatpak

Temperature Ranges
C = 0°C to +85°C. Case

Optional Processing
QR = 160 Hour Burn in

FAIRCHILD
A Schlumberger Company

F100415
1024 x 1-Bit Static Random Access Memory

Memory and High Speed Logic

Description

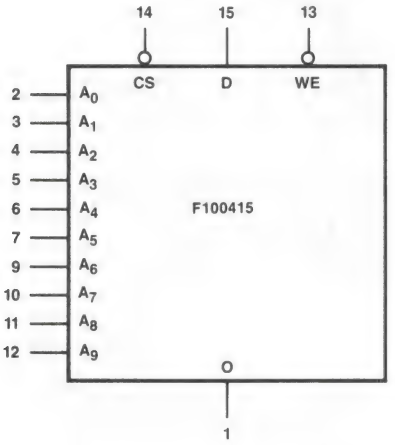
The F100415 is a 1024-bit read/write Random Access Memory (RAM), organized as 1024 words by one bit per word and designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data Input and non-inverting Data Output lines, as well as an active-LOW Chip Select line.

- **Address Access Time — 10 ns Max**
- **Chip Select Access Time — 5.0 ns Max**
- **Open-emitter Output for Easy Memory Expansion**
- **Power Dissipation — 0.79 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**
- **Polyimide Die Coat for Alpha Immunity**

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{CS}$	Chip Select Input (Active LOW)
A_0–A_9	Address Inputs
D	Data Input
O	Data Output

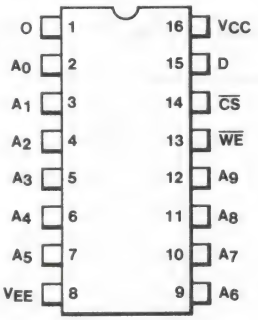
Logic Symbol



V_{CC} = Pin 16
V_{EE} = Pin 8

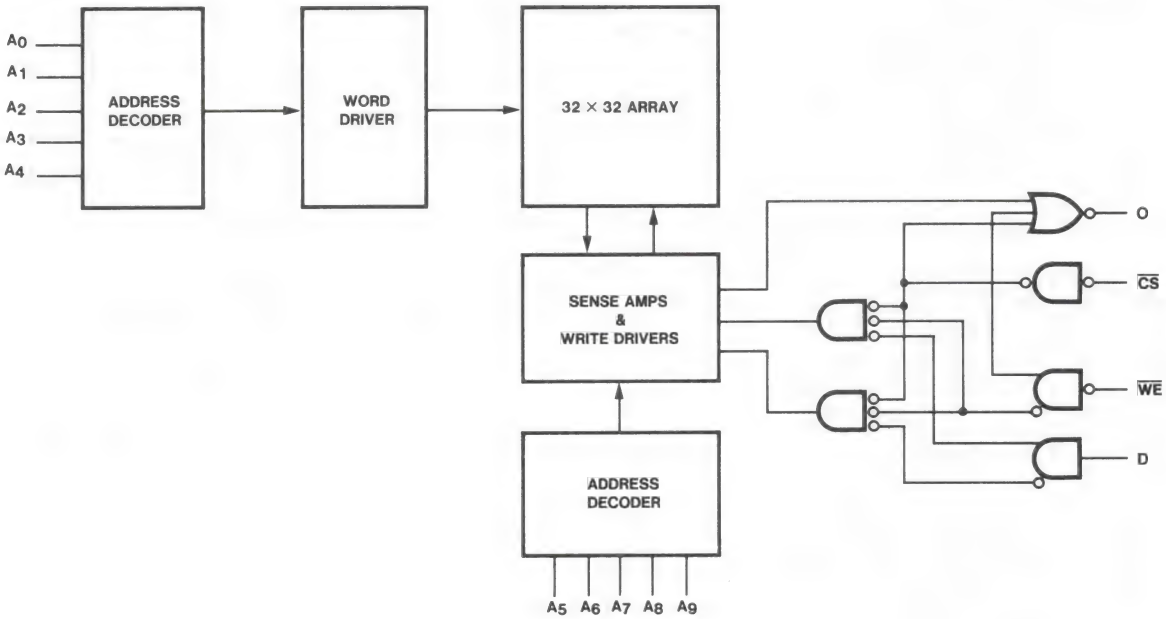
Connection Diagram

16-Pin DIP (Top View)



Note
The 16-pin Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package

Logic Diagram



Functional Description

The F100415 is a fully decoded 1024-bit read/write random access memory, organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A_0 through A_9.

One Chip Select input is provided for memory array expansion up to 2048 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of Chip Select, ($\overline{CS}$) from the address without affecting system performance.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at D is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the output (O).

The output of the F100415 is an unterminated emitter follower, which allows maximum flexibility in choosing output connection configurations. In many applications it is desirable to tie the outputs of several F100415 devices together to allow easy expansion. In other applications the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output.

Truth Table

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	D	O	
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Data	Read

H = HIGH Voltage Levels = −0.9 V (Nominal)
L = LOW Voltage Levels = −1.7 V (Nominal)
X = Don't Care
Data = Previously stored data

DC Performance Characteristic: V_{EE} = −4.2 V to −4.8 V, V_{CC} = GND, T_C = 0°C to +85°C unless otherwise specified[1]

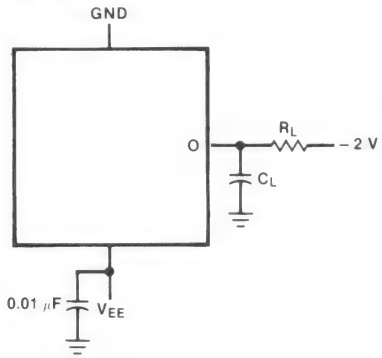
Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current			220	μA	$V_{IN} = V_{IH(max)}$
I_{IL}	Input LOW Current, $\overline{CS}$ $\overline{WE}$, A_0–A_9, D	0.5 −50		170	μA	$V_{IN} = V_{IL(min)}$
I_{EE}	Power Supply Current	−200	−180		mA	Inputs and Output Open

AC Performance Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = GND, Output Load = 50 Ω and 3 pF to -2.0 V, T_C = 0° C to +85° C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
	Read Timing					
t_{ACS}	Chip Select Access Time			5.0	ns	
t_{RCS}	Chip Select Recovery Time			5.0	ns	*Figures 3a, 3b*
t_{AA}	Address Access Time[2]			10	ns	
	Write Timing					
t_W	Write Pulse Width to Guarantee Writing[3]	7			ns	
t_{WSD}	Data Setup Time prior to Write	1.0			ns	
t_{WHD}	Data Hold Time after Write	2.0			ns	
t_{WSA}	Address Setup Time prior to Write[3]	1.0			ns	*Figure 4*
t_{WHA}	Address Hold Time after Write	2.0			ns	
t_{WSCS}	Chip Select Setup Time prior to Write	1.0			ns	
t_{WHCS}	Chip Select Hold Time after Write	2.0			ns	
t_{WS}	Write Disable Time			5.0	ns	
t_{WR}	Write Recovery Time			10	ns	
t_r	Output Rise Time		0.7		ns	Measured between 20% and
t_f	Output Fall Time		0.7		ns	80% or 80% and 20%
C_{IN}	Input Pin Capacitance		4.0	5.0	pF	Measured with a Pulse
C_{OUT}	Output Pin Capacitance		7.0	8.0	pF	Technique

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
3. t_W measured at t_{WSA} = Min, t_{WSA} measured at t_W = Min.

Fig. 1 AC Test Circuit



Notes

All Timing Measurements Referenced to 50% of Input Levels

C_L = 3 pF including Fixture and Stray Capacitance

R_L = 50 Ω to – 2.0 V.

Fig. 2 Input Levels

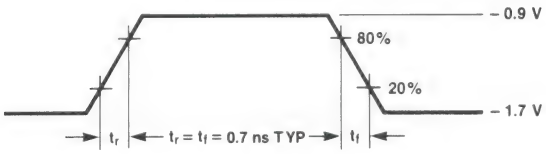
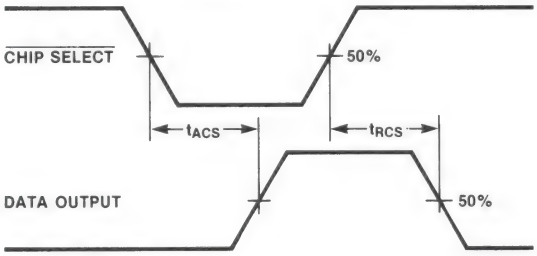
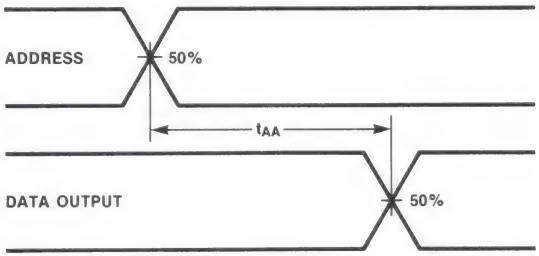


Fig. 3 Read Mode Timing

3a Read Mode Propagation Delay from Chip Select

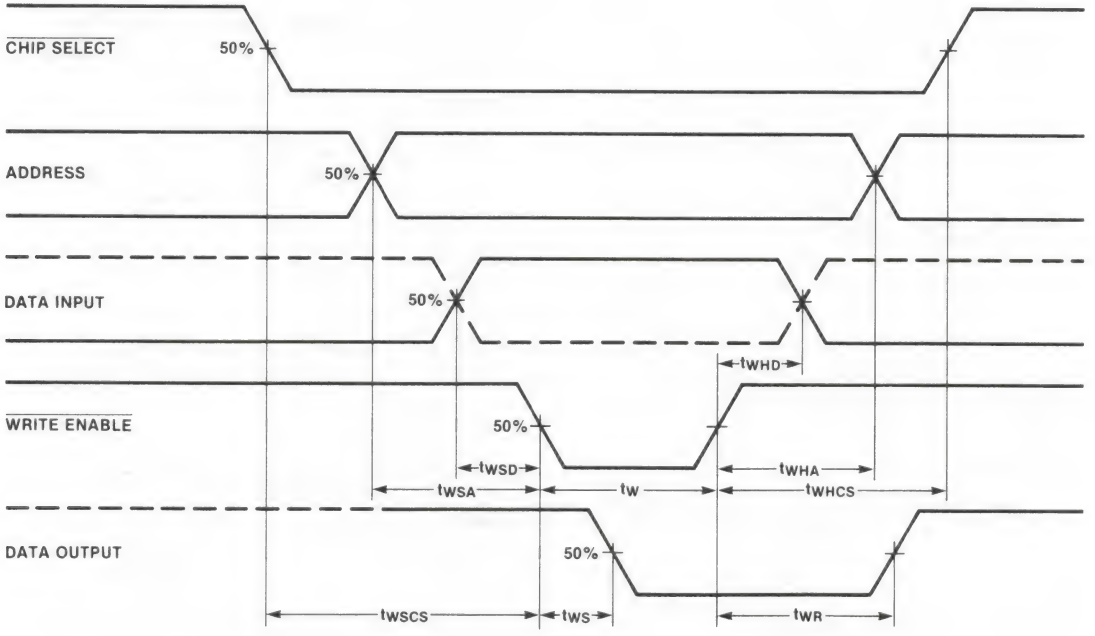


3b Read Mode Propagation Delay from Address



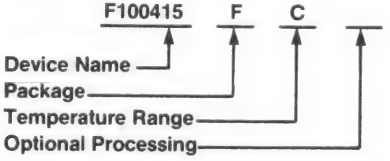
3

Fig. 4 Write Mode Timing



Note
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

Ordering Information



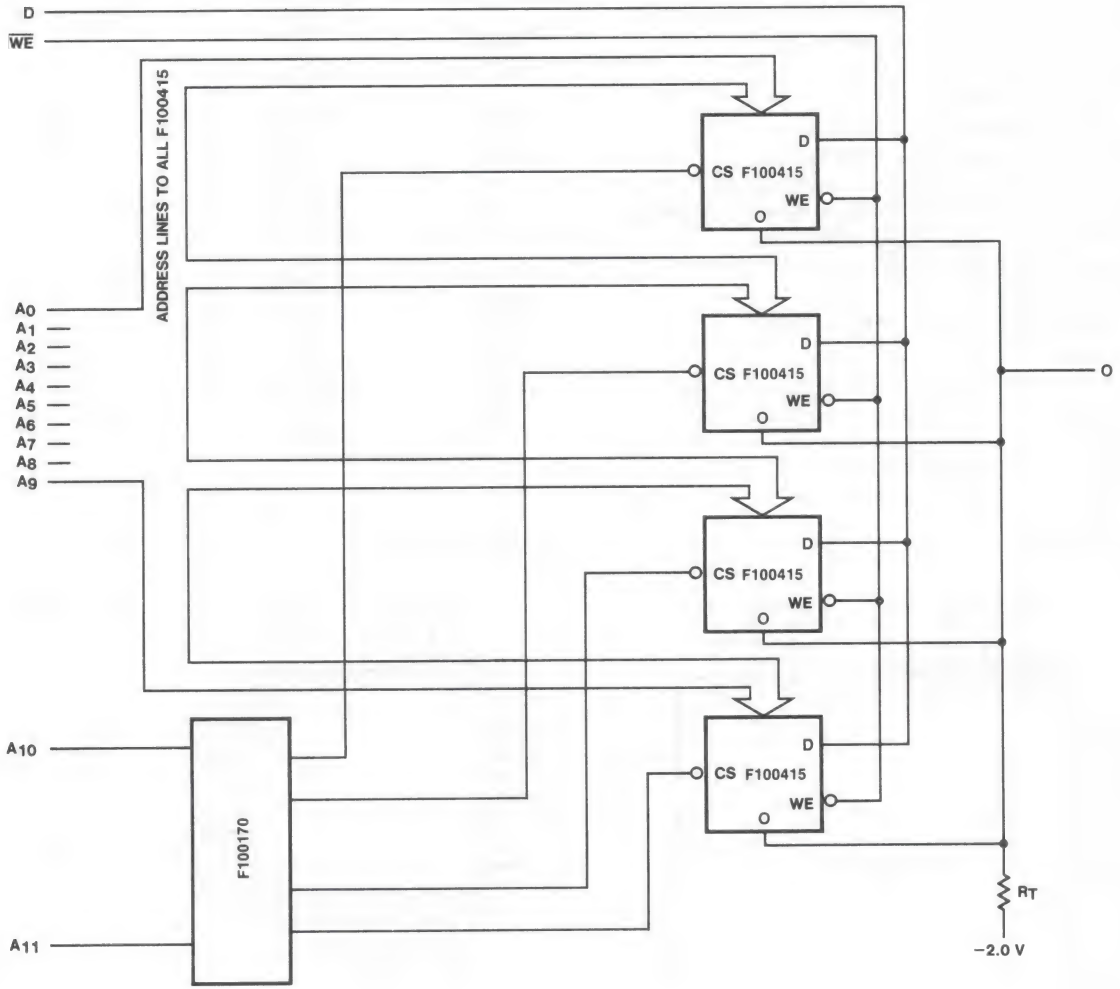
Packages and Outlines (See Section 9)
D = Ceramic DIP
F = Flatpak

Temperature Range
C = 0°C to +85°C, Case

Optional Processing
QR = 160 Hour Burn In or Equivalent

Typical Application

4096-Word x n-Bit System



FAIRCHILD
A Schlumberger Company

F100422
256 x 4-Bit Static Random Access Memory

Memory and High Speed Logic

Description

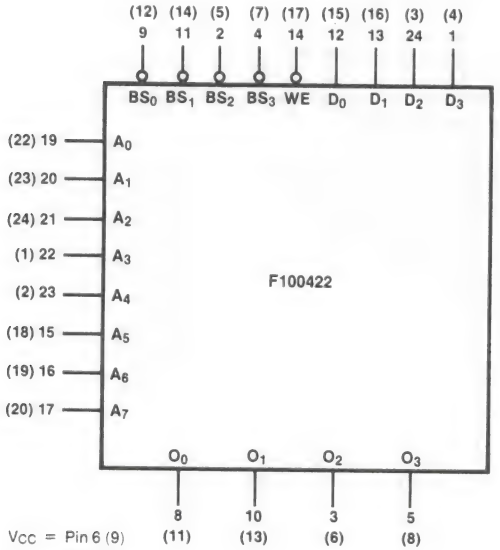
The F100422 is a 1024-bit read/write Random Access Memory (RAM), organized 256 words by four bits per word. It is designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as four active-LOW Bit Select lines.

- **Address Access Time — 10 ns Max**
- **Bit Select Access Time — 5.0 ns Max**
- **Four Bits Can be Independently Selected**
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation — 0.88 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**
- **Polyimide Die Coat for Alpha Immunity**

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{BS}_0 - \overline{BS}_3$	Bit Select Inputs (Active LOW)
$A_0 - A_7$	Address Inputs
$D_0 - D_3$	Data Inputs
$O_0 - O_3$	Data Outputs

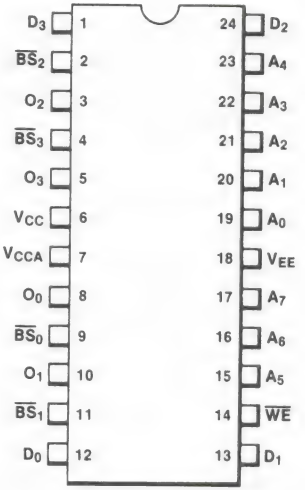
Logic Symbol



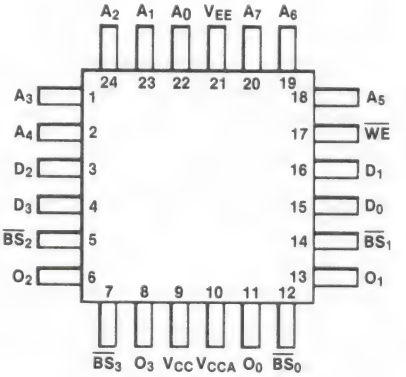
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Connection Diagrams

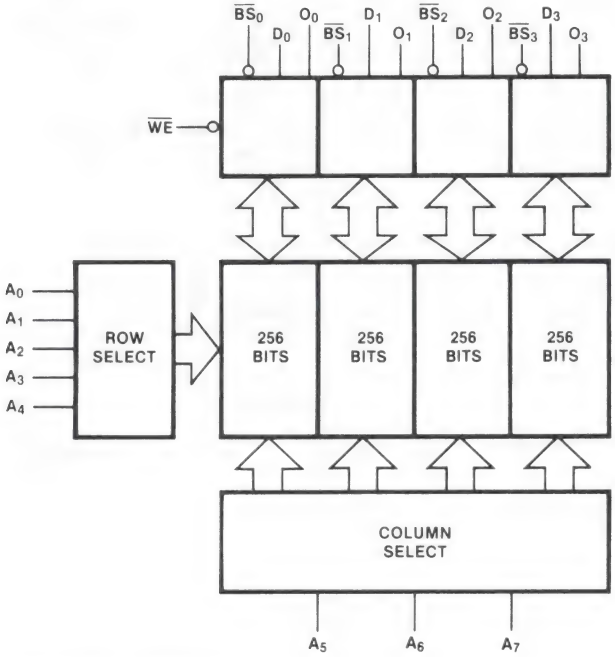
24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



Logic Diagram



Functional Description

The F100422 is a fully decoded 1024-bit read/write random access memory, organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, A_0 through A_7.

Four Bit Select inputs are provided for logic flexibility. For larger memories, the fast bit select access time permits the decoding of individual bit selects from the address without increasing address access time.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the bit selected, the data at D_0–D_3 is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the bit selected. Non-inverted data is then presented at the output (O_0–O_3).

The outputs of the F100422 are unterminated emitter followers, which allow maximum flexibility in choosing output connection configurations. In many applications it is desirable to tie the outputs of several F100422 devices together to allow easy expansion. In other applications the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output.

Truth Table

Inputs			Outputs	
$\overline{BS_n}$	$\overline{WE}$	D_n	O_n	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Data	Read

Each bit has independent $\overline{BS}$, D, and O, but all have common $\overline{WE}$
H = HIGH Voltage Levels = −0.9 V (Nominal)
L = LOW Voltage Levels = −1.7 V (Nominal)
X = Don't Care
Data = Previously stored data

DC Performance Characteristic: $V_{EE} = -4.2$ to -4.8 V, $V_{CC} = V_{CCA} = GND$, $T_C = 0°C$ to $+85°C$ unless otherwise specified[1]

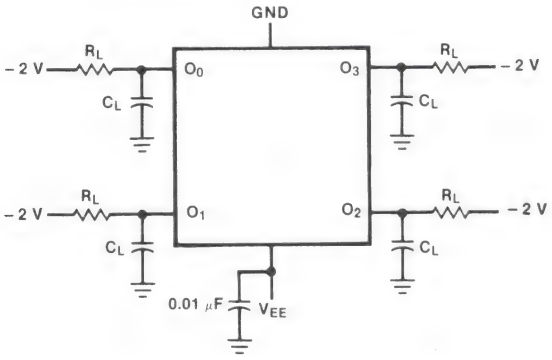
Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current			220	μA	$V_{IN} = V_{IH(max)}$
I_{IL}	Input LOW Current, $\overline{BS_0}$-$\overline{BS_3}$ $\overline{WE}$, A_0-A_7, D_0-D_3	0.5 −50		170	μA	$V_{IN} = V_{IL(min)}$
I_{EE}	Power Supply Current	-230	-200		mA	All Inputs and Outputs Open

AC Performance Characteristics: $V_{EE} = -4.2$ V to -4.8 V, $V_{CC} = V_{CCA} = GND$, Output Load = 50 Ω and 3 pF to -2.0 V, $T_C = 0°C$ to $+85°C$

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
	Read Timing					
t_{ABS}	Bit Select Access Time			5.0	ns	
t_{RBS}	Bit Select Recovery Time			5.0	ns	*Figures 3a, 3b*
t_{AA}	Address Access Time[2]			10	ns	
	Write Timing					
t_W	Write Pulse Width to Guarantee Writing[3]	7.0			ns	
t_{WSD}	Data Setup Time prior to Write	1.0			ns	
t_{WHD}	Data Hold Time after Write	2.0			ns	
t_{WSA}	Address Setup Time prior to Write[3]	1.0			ns	*Figure 4*
t_{WHA}	Address Hold Time after Write	2.0			ns	
t_{WSBS}	Bit Select Setup Time prior to Write	1.0			ns	
t_{WHBS}	Bit Select Hold Time after Write	2.0			ns	
t_{WS}	Write Disable Time			5.0	ns	
t_{WR}	Write Recovery Time			10	ns	
t_r	Output Rise Time		0.7		ns	Measured between 20% and
t_f	Output Fall Time		0.7		ns	80% or 80% and 20%
C_{IN}	Input Pin Capacitance		4.0	5.0	pF	Measured with a Pulse
C_{OUT}	Output Pin Capacitance		7.0	8.0	pF	Technique

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
3. t_W measured at t_{WSA} = Min, t_{WSA} measured at t_W = Min.

Fig. 1 AC Test Circuit



Notes
All Timing Measurements Referenced to 50% of Input Levels
C_L = 3 pF including Fixture and Stray Capacitance
R_L = 50 Ω to -2.0 V

Fig. 2 Input Levels

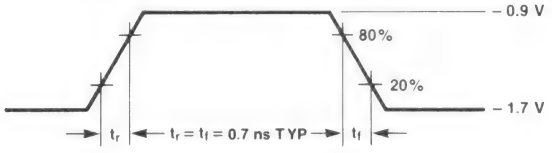
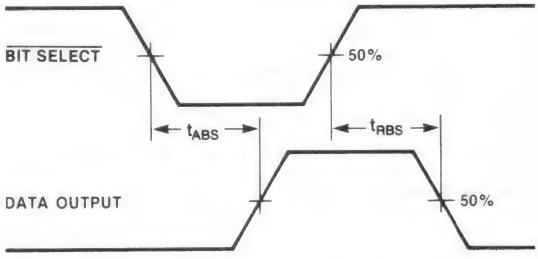
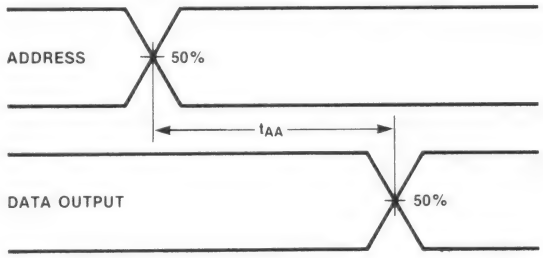


Fig. 3 Read Mode Timing

3a Read Mode Propagation Delay from Bit Select

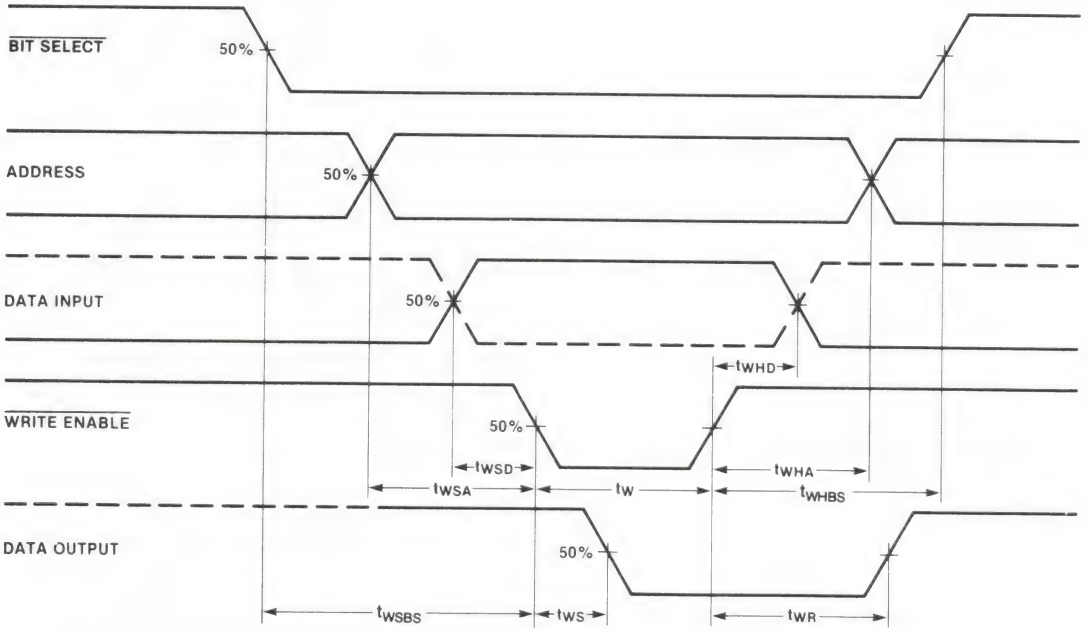


3b Read Mode Propagation Delay from Address



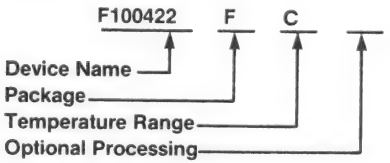
3

Fig. 4 Write Mode Timing



Note
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

Ordering Information



Packages and Outlines (See Section 9)
D = Ceramic DIP
F = Flatpak

Temperature Ranges
C = 0°C to +85°C, Case

Optional Processing
QR = 160 Hour Burn In

FAIRCHILD
A Schlumberger Company

F100422
256 x 4-Bit Static Random Access Memory

Memory and High Speed Logic

Description

The F100422 is a 1024-bit read/write Random Access Memory (RAM), organized 256 words by four bits per word. It is designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as four active-LOW Bit Select lines.

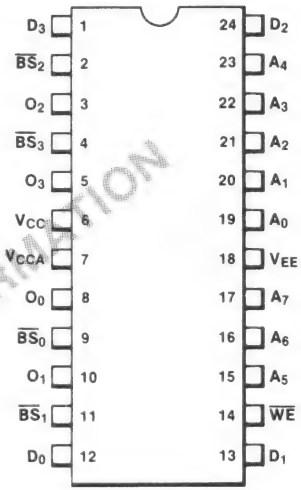
- **Address Access Times — 5/7 ns Max**
- **Bit Select Access Times — 4/5 ns Max**
- **Four Bits Can be Independently Selected**
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation — 0.88 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**
- **Polyimide Die Coat for Alpha Immunity**

Pin Names

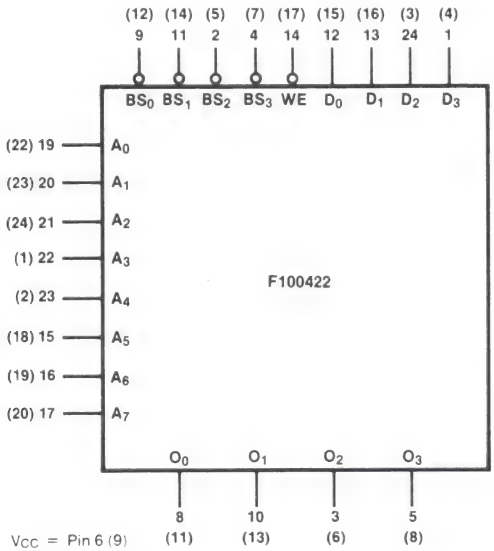
$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{BS}_0 - \overline{BS}_3$	Bit Select Inputs (Active LOW)
$A_0 - A_7$	Address Inputs
$D_0 - D_3$	Data Inputs
$O_0 - O_3$	Data Outputs

Connection Diagrams

24-Pin DIP (Top View)

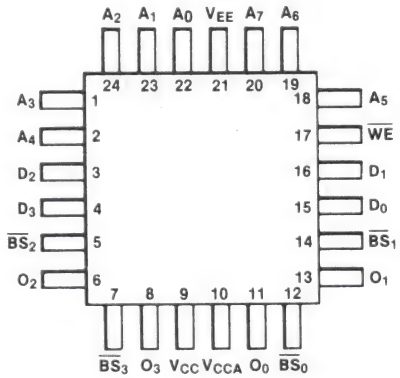


Logic Symbol



VCC = Pin 6 (9)
VCCA = Pin 7 (10)
VEE = Pin 18 (21)
( ) = Flatpak

24-Pin Flatpak (Top View)



3

FAIRCHILD
A Schlumberger Company

F100474
1024 x 4-Bit Static Random Access Memory

Memory and High Speed Logic

Description

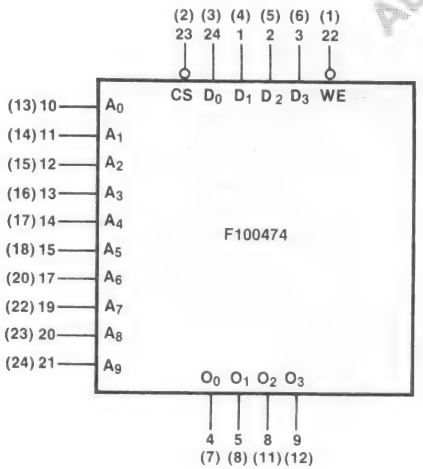
The F100474 is a 4096-bit read/write Random Access Memory (RAM), organized 1024 words by four bits per word. It is designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an active-LOW Chip Select line.

- **Address Access Time — 10 ns Max**
- **Chip Select Access Time — 5.0 ns Max**
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation — 0.25 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{CS}$	Chip Select Input (Active LOW)
A_0–A_9	Address Inputs
D_0–D_3	Data Inputs
O_0–O_3	Data Outputs

Logic Symbol

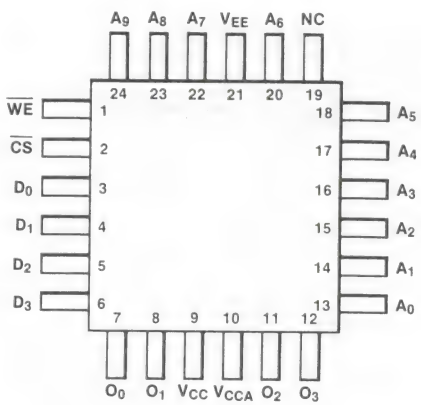


V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

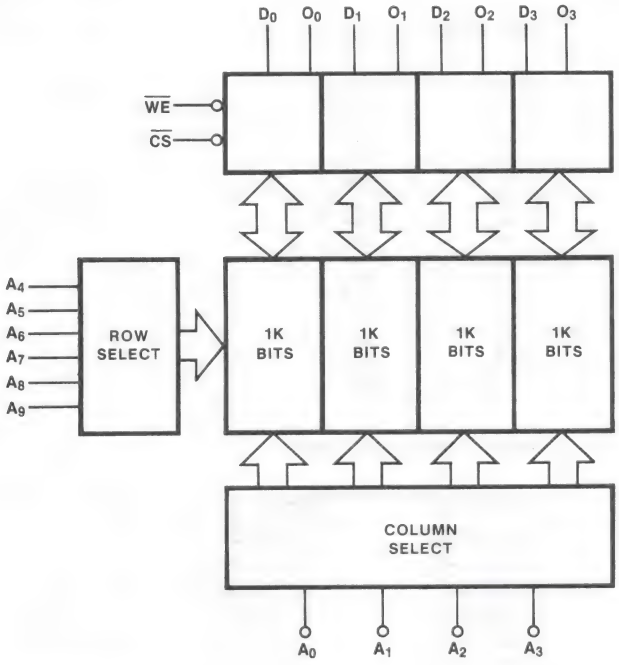
Connection Diagrams

24-Pin DIP (Top View)

24-Pin Flatpak (Top View)



Logic Diagram



Functional Description

The F100474 is a fully decoded 4096-bit read/write random access memory, organized 1024 words by four bits. Word selection is achieved by means of a 10-bit address, A_0 through A_9.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at D_0-D_3 is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the outputs (O_0-O_3).

The output of the F100474 is an unterminated emitter follower, which allows maximum flexibility in choosing connection configurations. In many applications such as memory expansion, the outputs of many F100474 devices can be tied together. In other applications the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is OFF.

Truth Table

Inputs			Outputs	
$\overline{CS}$	$\overline{WE}$	D_n	O_n	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Data	Read

H = HIGH Voltage Levels = −0.9 V (Nominal)
L = LOW Voltage Levels = −1.7 V (Nominal)
X = Don't Care
Data = Previously stored data

FAIRCHILD
A Schlumberger Company

F10145A
16 x 4 Register File (RAM)

Memory and High Speed Logic

Description

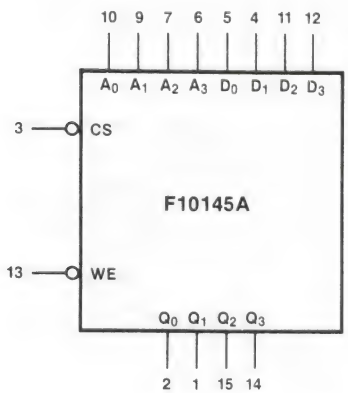
The F10145A is a high-speed 64-bit Random Access Memory organized as a 16-word by 4-bit array. External logic requirements are minimized by internal address decoding, while memory expansion and data bussing are facilitated by the output disabling features of the Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) inputs.

A HIGH signal on $\overline{CS}$ prevents read and write operations and forces the outputs to the LOW state. When $\overline{CS}$ is LOW, the $\overline{WE}$ input controls chip operations. A HIGH signal on $\overline{WE}$ disables the Data input (D_n) buffers and enables readout from the memory location determined by the Address (A_n) inputs. A LOW signal on $\overline{WE}$ forces the Q_n outputs LOW and allows data on the D_n inputs to be stored in the addressed location. Data exists in the same logical sense as presented at the data inputs, *i.e.*, the memory is non-inverting.

Pin Names

$\overline{CS}$	Chip Select
$A_0 - A_3$	Address
$D_0 - D_3$	Data Inputs
$\overline{WE}$	Write Enables
$Q_0 - Q_3$	Data Outputs

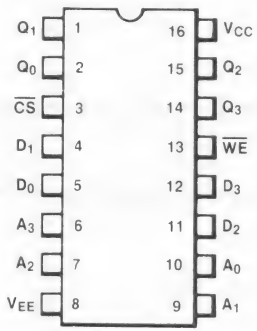
Logic Symbol



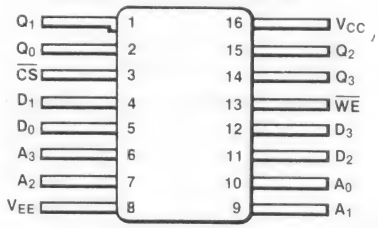
V_{CC} = Pin 16
V_{EE} = Pin 8

Connection Diagrams

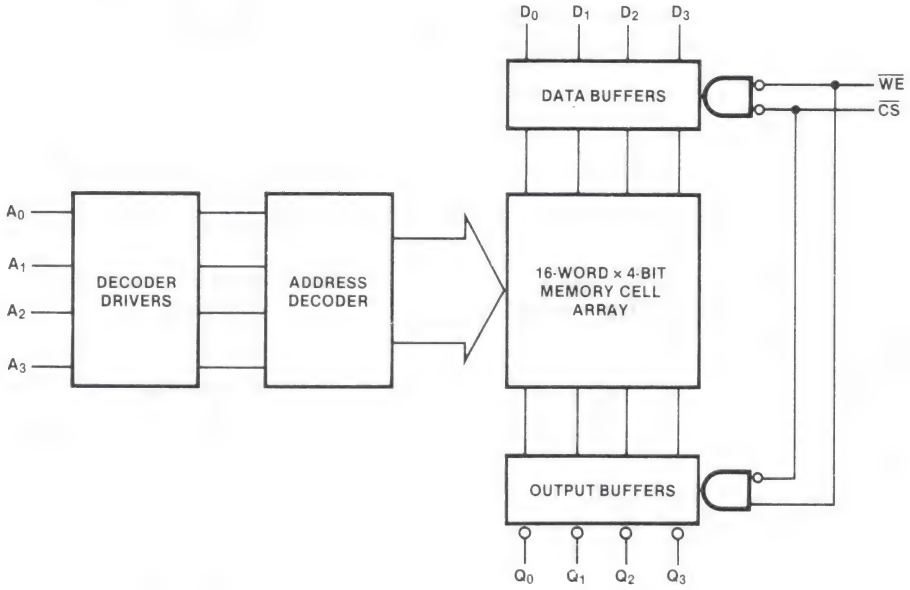
16-Pin DIP (Top View)



16-Pin Flatpak (Top View)



Logic Diagram



3

Fig. 1 AC Test Circuit

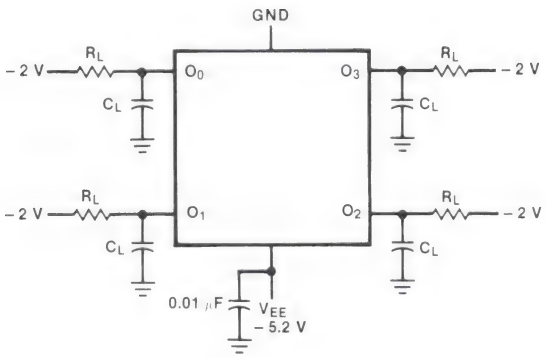
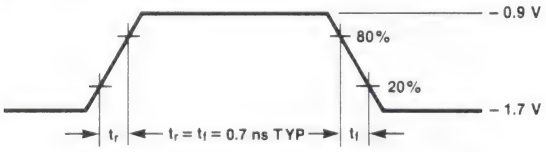


Fig. 2 Input Levels



Notes
All Timing Measurements Referenced to 50% of Input Levels
C_L = 3 pF including Fixture and Stray Capacitance
R_L = 50 Ω to –2.0 V

DC Performance Characteristics: $V_{EE} = -5.2$ V, V_{CC} = GND, $T_C = 0°C$ to $+75°C$[1]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current $\overline{CS}$, $A_0 - A_3$ $\overline{WE}$, $D_0 - D_3$			200 220	μA	$V_{IN} = V_{IH(max)}$
I_{EE}	Power Supply Current	−150	−100		mA	Inputs and Outputs Open

AC Performance Characteristics: $V_{EE} = -5.2$ V ±5%, V_{CC} = GND, $T_C = 0°C$ to $+75°C$

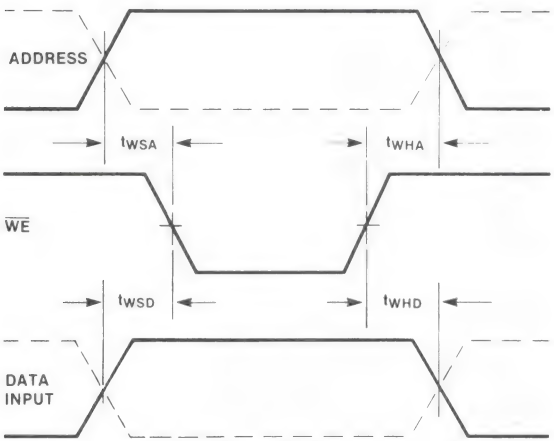
Symbol	Characteristic	Min	Typ	Max	Unit	Condition
	Access/Recovery Times					
t_{ACS}	Chip Select Access		4.5	6.0	ns	
t_{RCS}	Chip Select Recovery		4.5	6.0	ns	*Figures 1 and 4*
t_{AA}	Address Access[2]		6.5	9.0	ns	
	Write Setup Times					
t_{WSD}	Data	4.5	3.0		ns	
t_{WSCS}	Chip Select	4.5	2.5		ns	
t_{WSA}	Address	3.5	1.5		ns	
	Write Hold Times					*Figures 1 and 3*
t_{WHD}	Data	0	−0.5		ns	
t_{WHCS}	Chip Select	0.5	0		ns	
t_{WHA}	Address	1.0	−1.0		ns	
t_{WR}	Write Recovery Time		4.5	6.0	ns	
t_{WS}	Write Disable Time		4.5	6.0	ns	*Figures 1 and 4*
t_W	Write Pulse Width, Min	4.0	2.5		ns	*Figures 1 and 3*
t_{CS}	Chip Select Pulse Width, Min	4.0	2.5		ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.5	2.5	3.9	ns	*Figures 1 and 4*

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudo random testing pattern.

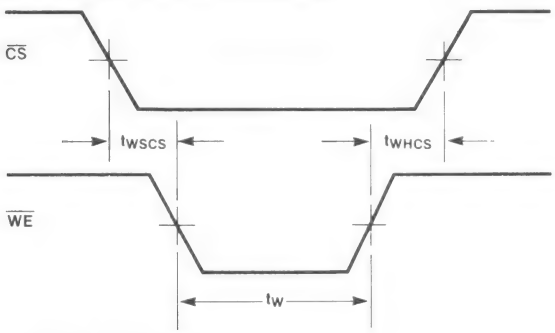
Fig. 3 **Write Modes**

Write Enable Strobe

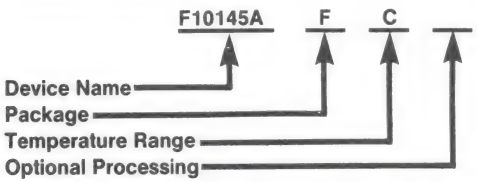
ADDRESS AND DATA INPUT SET-UP AND HOLD TIMES
($\overline{CS}$ = LOW)



CHIP SELECT SET-UP AND HOLD TIMES



Ordering Information



Packages and Outlines (See Section 9)
D = Ceramic DIP
F = Flatpak

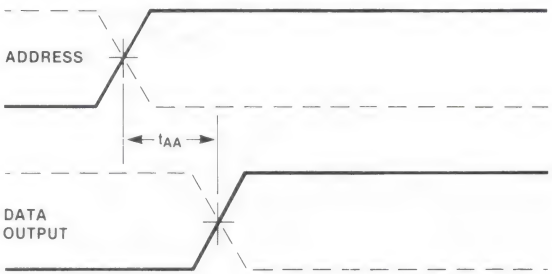
Temperature Ranges
C = 0° to + 75°C. Case

Optional Processing
QR = 160 Hour Burn in

Fig. 4 **Read Modes**

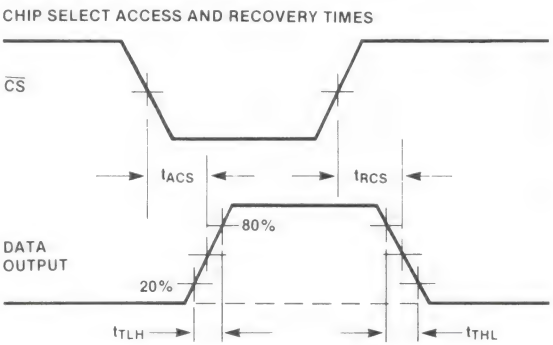
Address Input to Data Output ($\overline{WE}$ = HIGH, $\overline{CS}$ = LOW)

ADDRESS ACCESS TIME



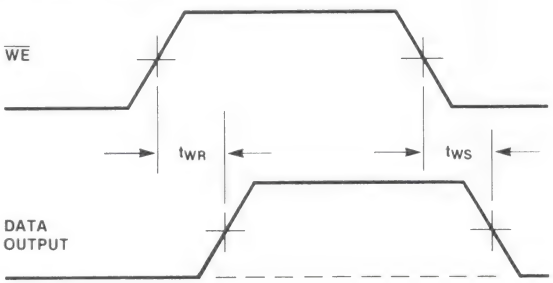
Chip Select Input to Data Output ($\overline{WE}$ = HIGH)

CHIP SELECT ACCESS AND RECOVERY TIMES



Write Enable Input to Data Output ($\overline{CS}$ = LOW)

WRITE RECOVERY, DISABLE TIMES



3

FAIRCHILD
A Schlumberger Company

F10402
16 x 4-Bit Register File (RAM)

Memory and High Speed Logic

Description

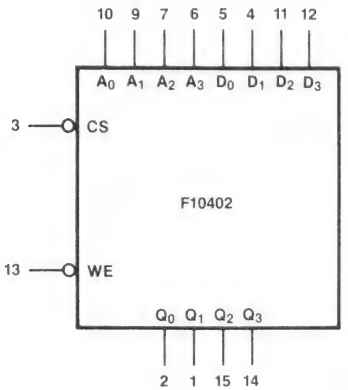
The F10402 is a high-speed 64-bit Random Access Memory (RAM) organized as a 16-word by 4-bit array. External logic requirements are minimized by internal address decoding, while memory expansion and data busing are facilitated by the output disabling features of the Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) inputs.

A HIGH signal on $\overline{CS}$ prevents read and write operations and forces the outputs to the LOW state. When $\overline{CS}$ is LOW, the $\overline{WE}$ input controls chip operations. A HIGH signal on $\overline{WE}$ disables the Data input (D_n) buffers and enables readout from the memory location determined by the Address (A_n) inputs. A LOW signal on $\overline{WE}$ forces the Q_n outputs LOW and allows data on the D_n inputs to be stored in the addressed location. Data exists in the same logical sense as presented at the data inputs, *i.e.*, the memory is non-inverting.

Pin Names

$\overline{CS}$	Chip Select Input
$A_0 - A_3$	Address Inputs
$D_0 - D_3$	Data Inputs
$\overline{WE}$	Write Enable Input
$Q_0 - Q_3$	Data Outputs

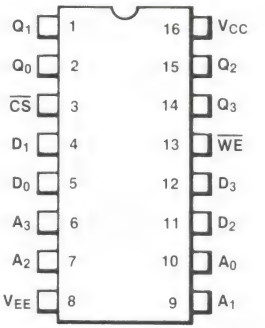
Logic Symbol



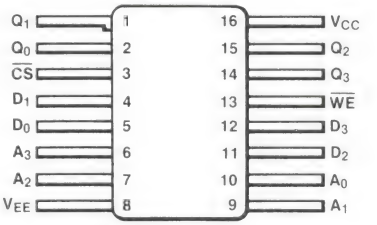
V_{CC} = Pin 16
V_{EE} = Pin 8

Connection Diagrams

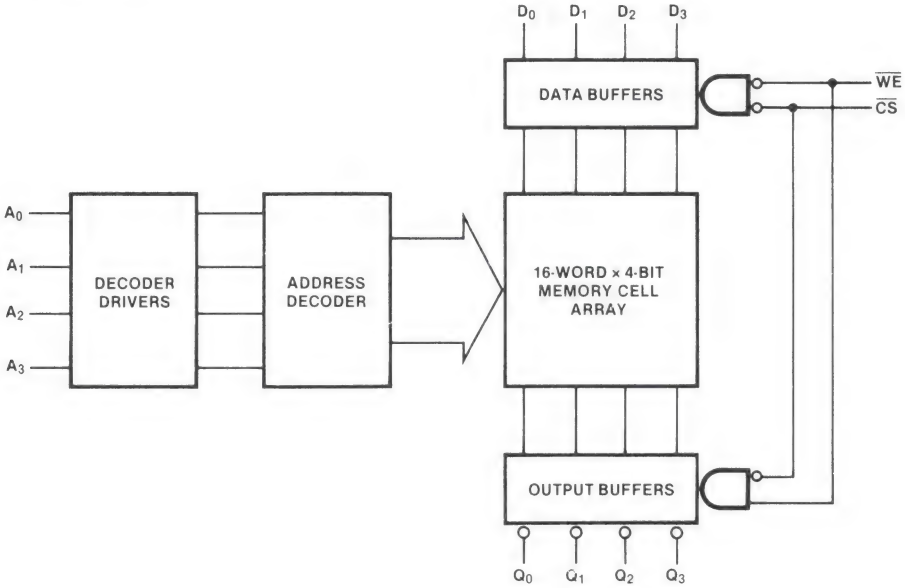
16-Pin DIP (Top View)



16-Pin Flatpak (Top View)



Logic Diagram



DC Performance Characteristics: $V_{EE} = -5.2$ V, $V_{CC} = V_{CCA} =$ GND, $T_C = 0°C$ to $+75°C$ unless otherwise specified*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current All Inputs			300	μA	$V_{IN} = V_{IH(max)}$
I_{EE}	Power Supply Current	−170	−110	−70	mA	Inputs Open

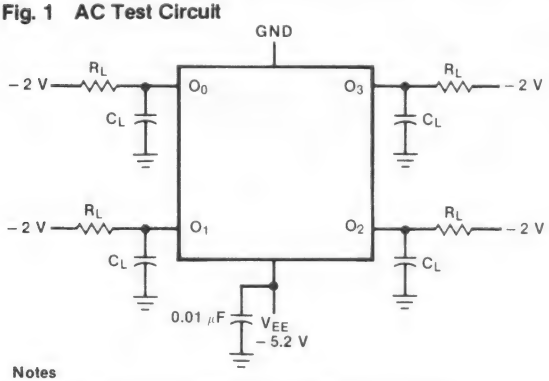
*See Family Characteristic for other dc specifications.

AC Performance Characteristics: $V_{EE} = -5.2\ V \pm 5\%$, V_{CC} = GND, Applies to Flatpack and DIP Packages

Symbol	Characteristic	$T_C = 0°C$ Min	$T_C = 0°C$ Max	$T_C = 25°C$ Min	$T_C = 25°C$ Max	$T_C = 75°C$ Min	$T_C = 75°C$ Max	Unit	Condition
	Access/Recovery Timing								
t_{ACS}	Chip Select Access		3.30		3.50		3.80	ns	
t_{RCS}	Chip Select Recovery		3.30		3.50		3.80	ns	*Figures 1 and 4*
t_{AA}	Address Access[1]		5.00		5.30		6.00	ns	
	Write Timing, Setup								
t_{WSD}	Data	0.50		0.50		0.80		ns	
t_{WSCS}	Chip Select	1.50		1.50		1.50		ns	
t_{WSA}	Address	1.00		1.00		1.00		ns	
	Write Timing, Hold								*Figures 1 and 3* $T_W = 6$ ns
t_{WHD}	Data	0.50		0.50		0.50		ns	
t_{WHCS}	Chip Select	0.50		0.50		0.50		ns	
t_{WHA}	Address	2.50		2.50		2.50		ns	
t_{WR}	Write Recovery Time		4.00		4.00		4.50	ns	
t_{WS}	Write Disable Time		3.00		3.00		3.50	ns	*Figures 1 and 4*
t_W	Write Pulse Width, (LOW)	2.50		2.50		3.00		ns	*Figures 1 and 3*
t_{CS}	Chip Select Pulse Width, (LOW)	2.50		2.50		3.00		ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	1.70	0.50	1.70	0.50	1.70	ns	*Figures 1 and 4*

1. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudo random testing pattern.

Fig. 1 AC Test Circuit



Notes
All Timing Measurments Referenced to 50% of Input Levels
C_L = 3 pF including Fixture and Stray Capacitance
R_L = 50 Ω to -2.0 V

Fig. 2 Input Levels

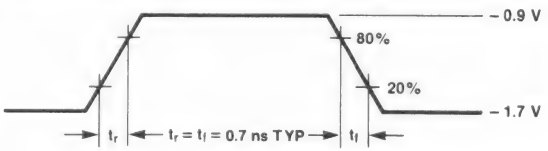
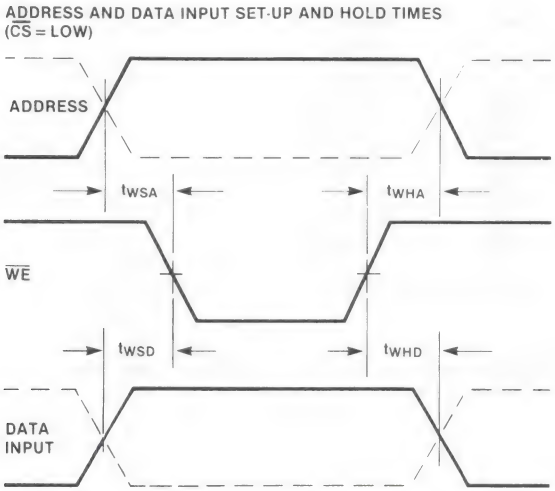
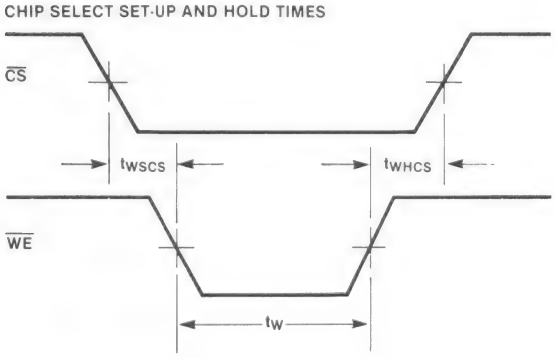


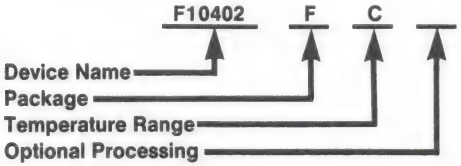
Fig. 3 Write Modes

Write Enable Strobe





Ordering Information



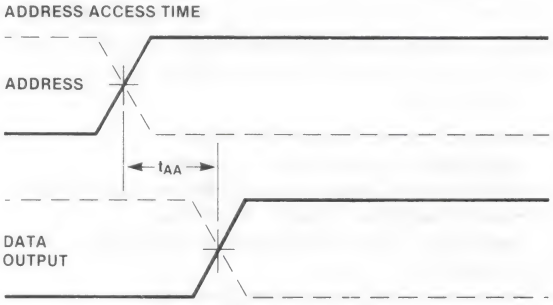
Packages and Outlines (See Section 9)
D = Ceramic DIP
F = Flatpak

Temperature Ranges
C = 0° to + 75°C. Case

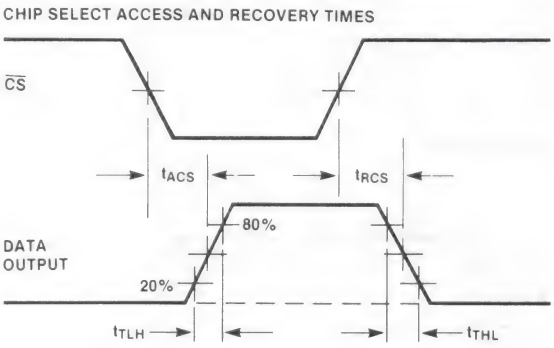
Optional Processing
QR = 160 Hour Burn in

Fig. 4 Read Modes

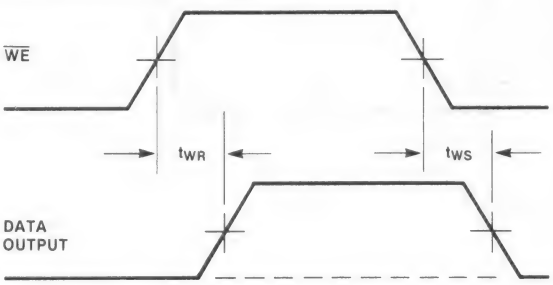
Address Input to Data Output ($\overline{WE}$ = HIGH, $\overline{CS}$ = LOW)



Chip Select Input to Data Output ($\overline{WE}$ = HIGH)



Write Enable Input to Data Output ($\overline{CS}$ = LOW)



FAIRCHILD
A Schlumberger Company

F10415
1024 x 1-Bit Static Random Access Memory

Memory and High Speed Logic

Description

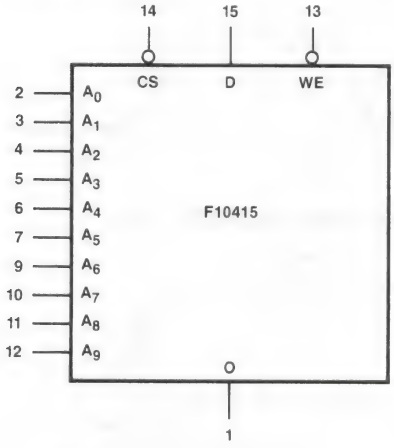
The F10415 is a 1024-bit read/write Random Access Memory (RAM), organized as 1024 words by one bit per word and designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an active-LOW Chip Select line.

- **Address Access Time — 10 ns Max**
- **Chip Select Access Time — 5 ns Max**
- **Open-emitter Output for Easy Memory Expansion**
- **Power Dissipation — 0.92 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**
- **Polyimide Die Coat for Alpha Immunity**

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{CS}$	Chip Select Input (Active LOW)
A_0–A_9	Address Inputs
D	Data Input
O	Data Output

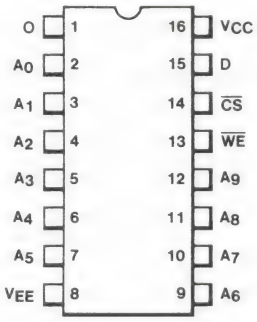
Logic Symbol



V_{CC} = Pin 16
V_{EE} = Pin 8

Connection Diagram

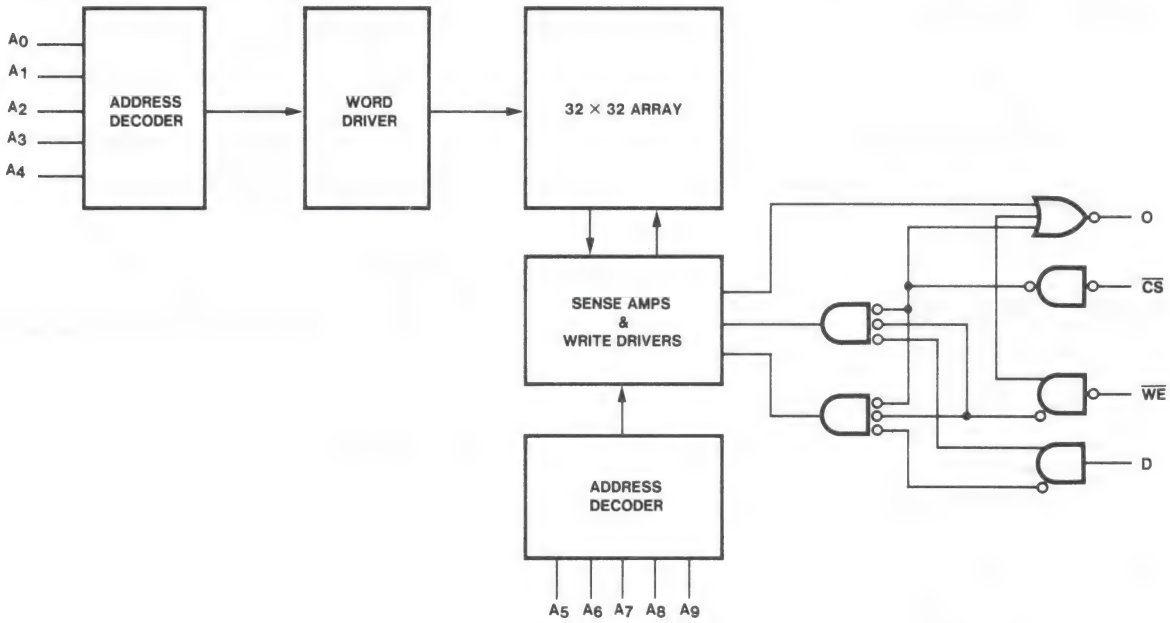
16-Pin DIP (Top View)



Note

The 16-pin Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package

Logic Diagram



Functional Description

The F10415 is a fully decoded 1024-bit read/write random access memory, organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A_0 through A_9.

One Chip Select input is provided for memory array expansion up to 2048 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of Chip Select, ($\overline{CS}$) from the address without affecting system performance.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at D is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the output (O).

The output of the F10415 is an unterminated emitter follower, which allows maximum flexibility in choosing output connection configurations. In many applications it is desirable to tie the outputs of several F10415 devices together to allow easy expansion. In other applications the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output.

Truth Table

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	D	O	
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Data	Read

H = HIGH Voltage Levels = −0.9 V (Nominal)
L = LOW Voltage Levels = −1.7 V (Nominal)
X = Don't Care
Data = Previously stored data

DC Performance Characteristic: $V_{EE} = -5.2$ V, V_{CC} = GND, $T_C = 0°C$ to $+75°C$ unless otherwise specified[1]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current			220	μA	$V_{IN} = V_{IH(max)}$
I_{IL}	Input LOW Current, $\overline{CS}$ $\overline{WE}$, A_0–A_9, D	0.5 −50		170	μA	$V_{IN} = V_{IL(min)}$
I_{EE}	Power Supply Current	−200	−180		mA	Inputs and Output Open

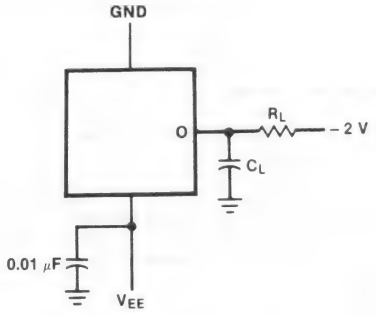
AC Performance Characteristics: $V_{EE} = -5.2$ V ± 5%, V_{CC} = GND, Output Load = 50 Ω and 3 pF to -2.0 V, $T_C = 0°C$ to $+75°C$

Symbol	Characteristic	F10415 Min	F10415 Max	Unit	Condition
	Read Timing				
t_{ACS}	Chip Select Access Time		5.0	ns	
t_{RCS}	Chip Select Recovery Time		5.0	ns	*Figures 3a, 3b*
t_{AA}	Address Access Time[2]		10	ns	
	Write Timing				
t_W	Write Pulse Width to Guarantee Writing[3]	7.0		ns	
t_{WSD}	Data Setup Time Prior to Write	1.0		ns	
t_{WHD}	Data Hold Time after Write	2.0		ns	
t_{WSA}	Address Setup Time Prior to Write[3]	1.0		ns	*Figure 4*
t_{WHA}	Address Hold Time after Write	2.0		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	1.0		ns	
t_{WHCS}	Chip Select Hold Time after Write	2.0		ns	
t_{WS}	Write Disable Time		5.0	ns	
t_{WR}	Write Recovery Time		10	ns	

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_r	Output Rise Time		0.7		ns	Measured between 20% and
t_f	Output Fall Time		0.7		ns	80% or 80% and 20%
C_{IN}	Input Pin Capacitance		4.0	5.0	pF	Measured with a Pulse
C_{OUT}	Output Pin Capacitance		7.0	8.0	pF	Technique

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
3. T_W measured at t_{WSA} = Min, t_{WSA} measured at t_W = Min.

Fig. 1 AC Test Circuit



Notes
All Timing Measurements Referenced to 50% of Input Levels
C_L = 3 pF including Fixture and Stray Capacitance
R_L = 50 Ω to –2.0 V

Fig. 2 Input Levels

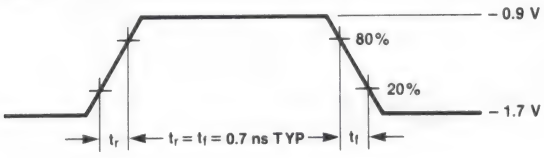
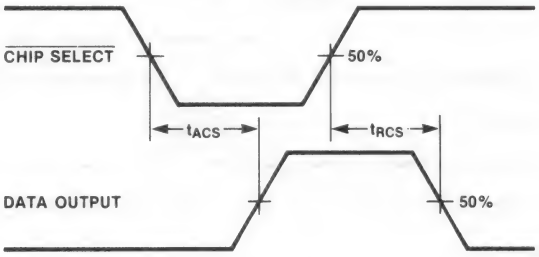
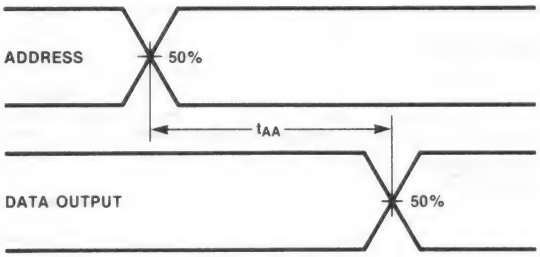


Fig. 3 Read Mode Timing

3a Read Mode Propagation Delay from Chip Select

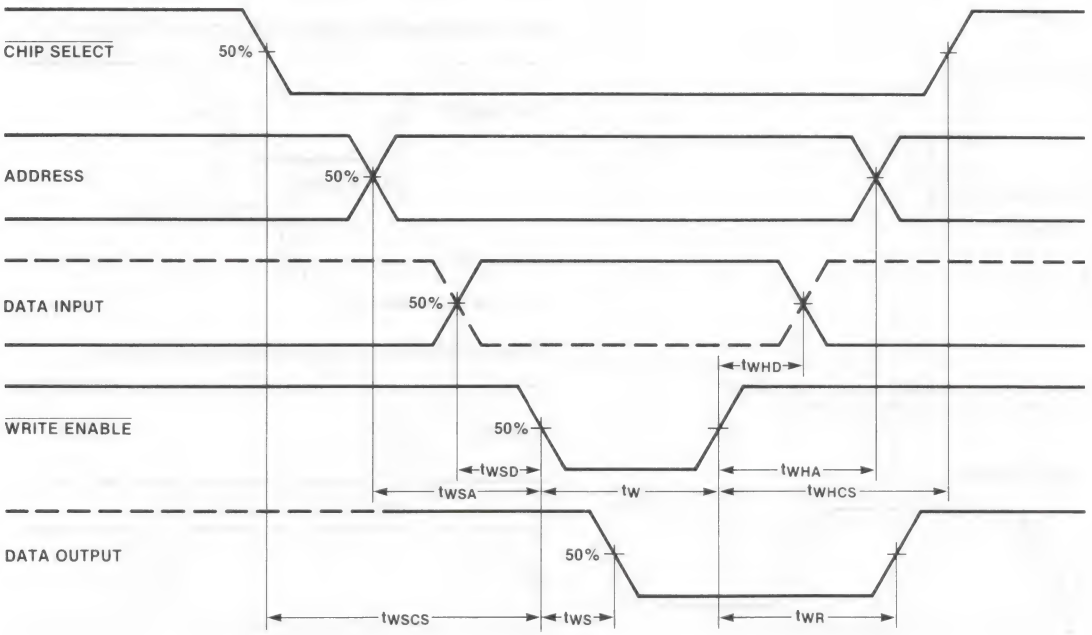


3b Read Mode Propagation Delay from Address



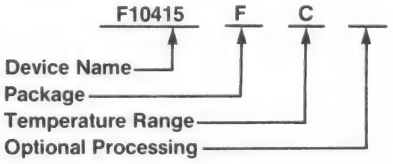
3

Fig. 4 Write Mode Timing



Note
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

Ordering Information



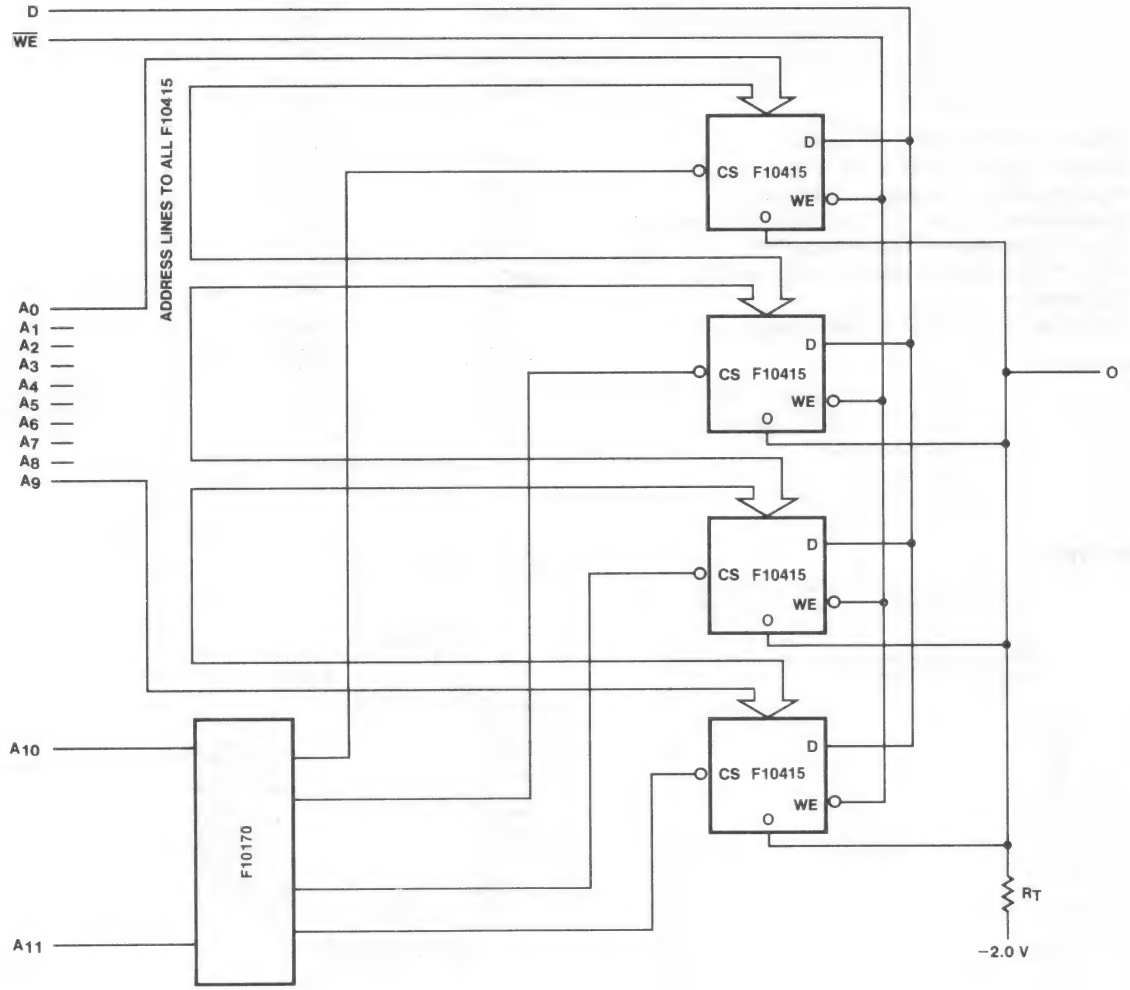
Packages and Outlines (See Section 9)
D = Ceramic DIP
F = Flatpak

Temperature Range
C = 0° C to +75° C, Case

Optional Processing
QR = 160 Hour Burn In

Typical Application

4096-Word x n-Bit System



FAIRCHILD
A Schlumberger Company

F10422
256 x 4-Bit Static Random Access Memory

Memory and High Speed Logic

Description

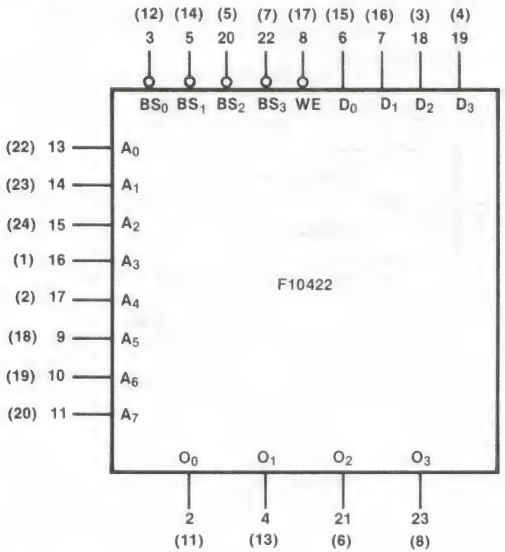
The F10422 is a 1024-bit read/write Random Access Memory (RAM), organized 256 words by four bits per word. It is designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as four active-LOW Bit Select lines.

- **Address Access Time — 10 ns Max**
- **Bit Select Access Time — 5.0 ns Max**
- **Four Bits Can be Independently Selected**
- **Open-emitter Output for Easy Memory Expansion**
- **Power Dissipation — 1.02 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**
- **Polyimide Die Coat for Alpha Immunity**

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{BS}_0 - \overline{BS}_3$	Bit Select Inputs (Active LOW)
$A_0 - A_7$	Address Inputs
$D_0 - D_3$	Data Inputs
$O_0 - O_3$	Data Outputs

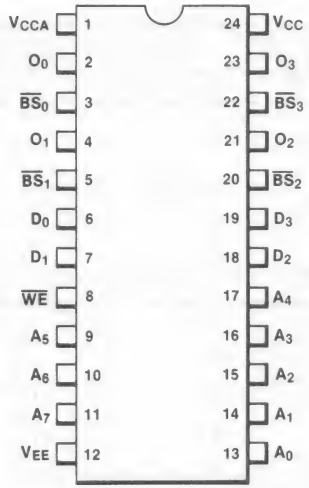
Logic Symbol



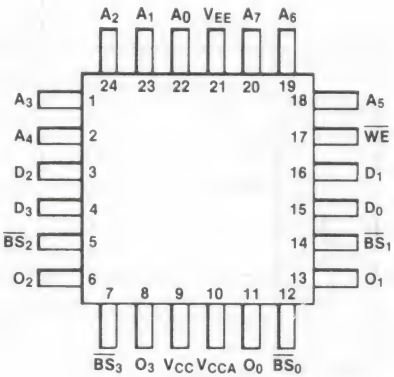
V_{CC} = Pin 24
V_{CCA} = Pin 1
V_{EE} = Pin 12
( ) = Flatpak

Connection Diagram

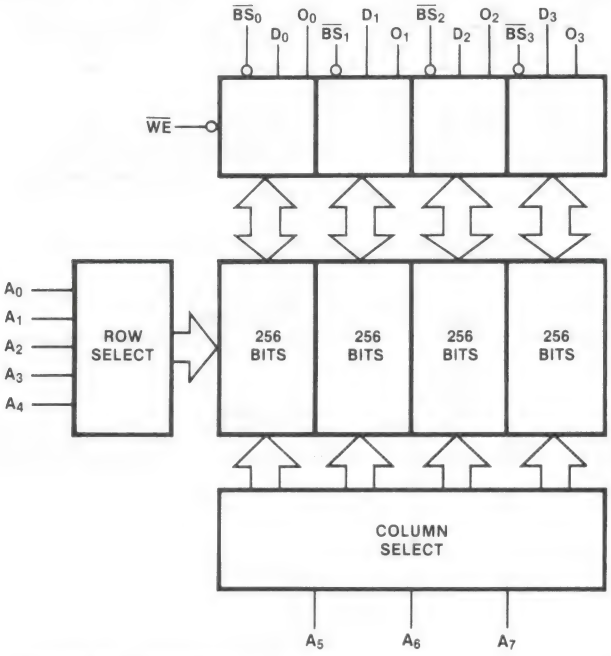
24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



Logic Diagram



Functional Description

The F10422 is a fully decoded 1024-bit read/write random access memory, organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, A_0 through A_7.

Four Bit Select inputs are provided for logic flexibility. For larger memories, the fast bit select access time permits the decoding of individual bit selects from the address without increasing address access time.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the bit selected, the data at D_0–D_3 is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the bit selected. Non-inverted data is then presented at the output (O_0–O_3).

The output of the F10422 is an unterminated emitter follower, which allows maximum flexibility in choosing output connection configurations. In many applications it is desirable to tie the outputs of several F10422 devices together to allow easy expansion. In other applications the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output.

Truth Table

Inputs			Outputs	
$\overline{BS}_n$	$\overline{WE}$	D_n	O_n	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Data	Read

Each bit has independent $\overline{BS}$, D, and O, but all have common $\overline{WE}$
H = HIGH Voltage Levels = −0.9 V (Nominal)
L = LOW Voltage Levels = −1.7 V (Nominal)
X = Don't Care
Data = Previously stored data

DC Performance Characteristic: $V_{EE} = -5.2$ V, $V_{CC} = V_{CCA} = GND$, $T_C = 0°C$ to $+75°C$ unless otherwise specified[1]

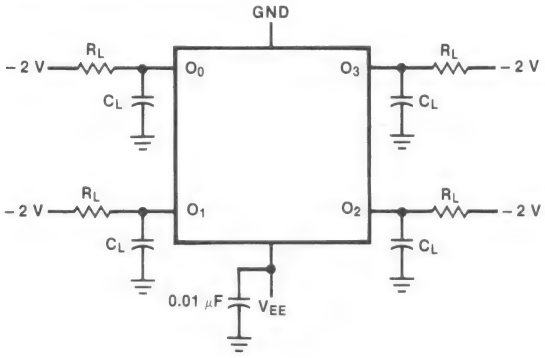
Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current			220	μA	$V_{IN} = V_{IH(max)}$
I_{IL}	Input LOW Current, $\overline{BS_0}$-$\overline{BS_3}$ $\overline{WE}$, A_0-A_7, D_0-D_3	0.5 −50		170	μA	$V_{IN} = V_{IL(min)}$
I_{EE}	Power Supply Current	-230	-200		mA	All Inputs and Outputs Open

AC Performance Characteristic: $V_{EE} = -5.2$ V ± 5%, $V_{CC} = V_{CCA} = GND$, Output Load = 50 Ω and 3 pF to -2.0 V, $T_C = 0°C$ to + 75° C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
	Read Timing					
t_{ABS}	Bit Select Access Time			5.0	ns	
t_{RBS}	Bit Select Recovery Time			5.0	ns	*Figures 3a, 3b*
t_{AA}	Address Access Time[2]			10	ns	
	Write Timing					
t_W	Write Pulse Width to Guarantee Writing[3]	7.0			ns	
t_{WSD}	Data Setup Time prior to Write	1.0			ns	
t_{WHD}	Data Hold Time after Write	2.0			ns	
t_{WSA}	Address Setup Time prior to Write[3]	1.0			ns	*Figure 4*
t_{WHA}	Address Hold Time after Write	2.0			ns	
t_{WSBS}	Bit Select Setup Time prior to Write	1.0			ns	
t_{WHBS}	Bit Select Hold Time after Write	2.0			ns	
t_{WS}	Write Disable Time			5.0	ns	
t_{WR}	Write Recovery Time			10	ns	
t_r	Output Rise Time		0.7		ns	Measured between 20% and
t_f	Output Fall Time		0.7		ns	80% or 80% and 20%
C_{IN}	Input Pin Capacitance		4.0	5.0	pF	Measured with a Pulse
C_{OUT}	Output Pin Capacitance		7.0	8.0	pF	Technique

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
3. t_W measured at t_{WSA} = Min, t_{WSA} measured at t_W = Min.

Fig. 1 AC Test Circuit



Notes
All Timing Measurements Referenced to 50% of Input Levels
C_L = 3 pF including Fixture and Stray Capacitance
R_L = 50 Ω to –2.0 V

Fig. 2 Input Levels

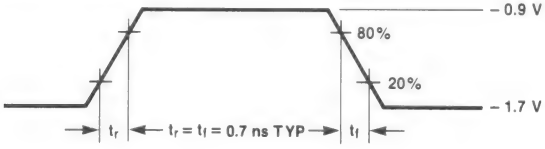
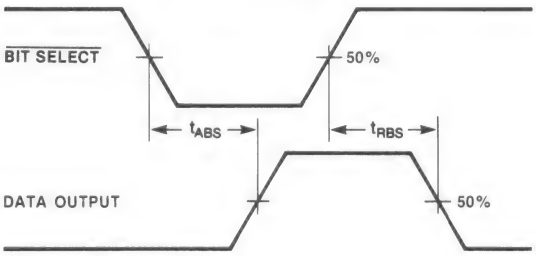
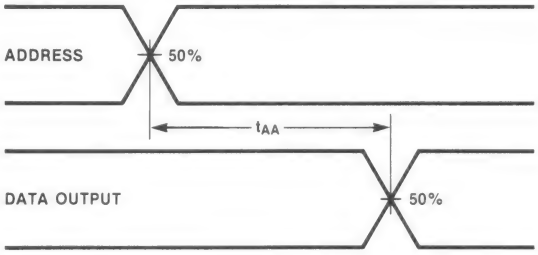


Fig. 3 Read Mode Timing

3a Read Mode Propagation Delay from Bit Select

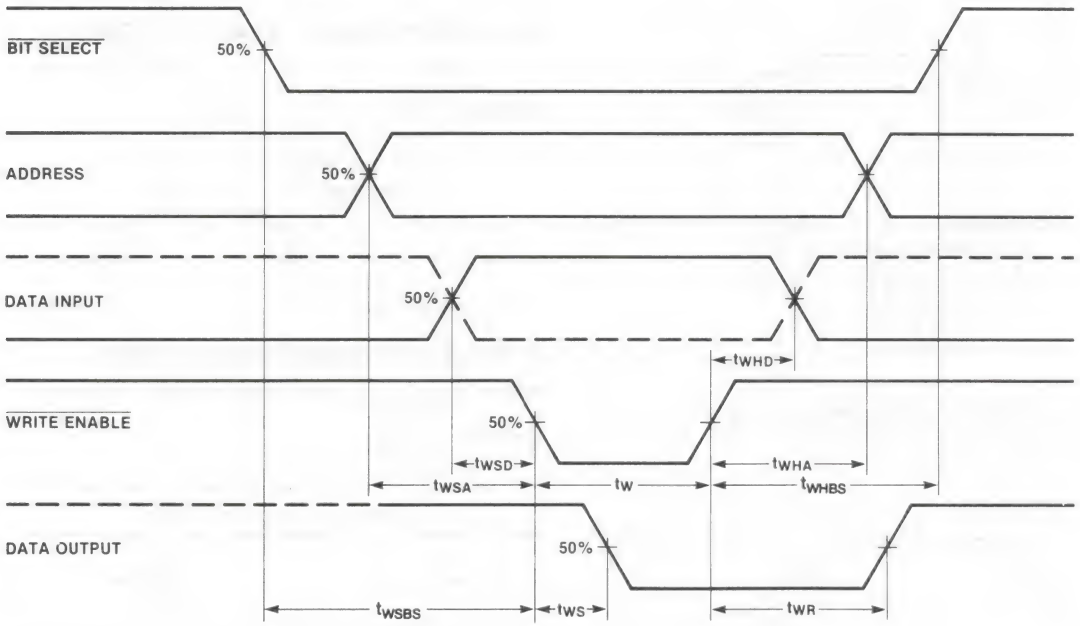


3b Read Mode Propagation Delay from Address



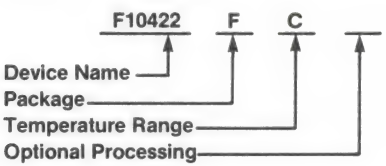
3

Fig. 4 Write Mode Timing



Note
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

Ordering Information



Packages and Outlines (See Section 9)
D = Ceramic DIP
F = Flatpak

Temperature Ranges
C = 0° C to +75° C, Case

Optional Processing
QR = 160 Hour Burn In

FAIRCHILD
A Schlumberger Company

F10422
256 x 4-Bit Static Random Access Memory

Memory and High Speed Logic

Description

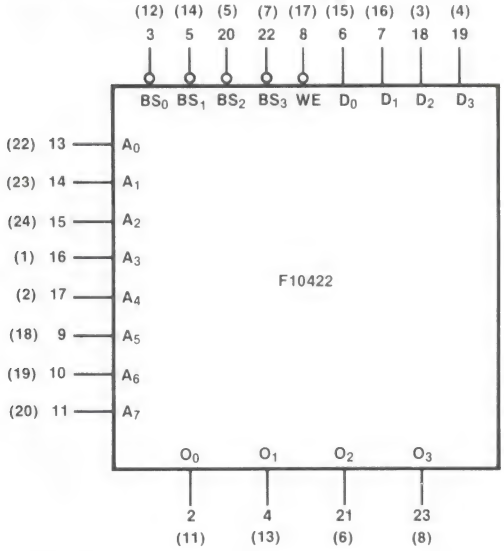
The F10422 is a 1024-bit read/write Random Access Memory (RAM), organized 256 words by four bits per word. It is designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as four active-LOW Bit Select lines.

- **Address Access Times — 5/7 ns Max**
- **Bit Select Access Times — 4/5 ns Max**
- **Four Bits Can be Independently Selected**
- **Open-emitter Output for Easy Memory Expansion**
- **Power Dissipation — 1.02 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**
- **Polyimide Die Coat for Alpha Immunity**

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{BS}_0 - \overline{BS}_3$	Bit Select Inputs (Active LOW)
$A_0 - A_7$	Address Inputs
$D_0 - D_3$	Data Inputs
$O_0 - O_3$	Data Outputs

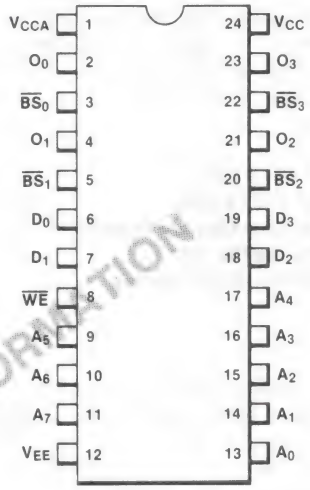
Logic Symbol



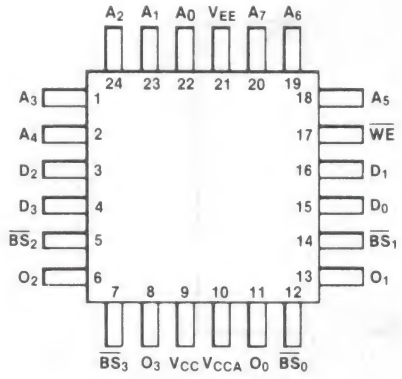
V_{CC} = Pin 24
V_{CCA} = Pin 1
V_{EE} = Pin 12
( ) Flatpak

Connection Diagram

24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



FAIRCHILD
A Schlumberger Company

F10474
1024 x 4-Bit Static Random Access Memory

Memory and High Speed Logic

Description

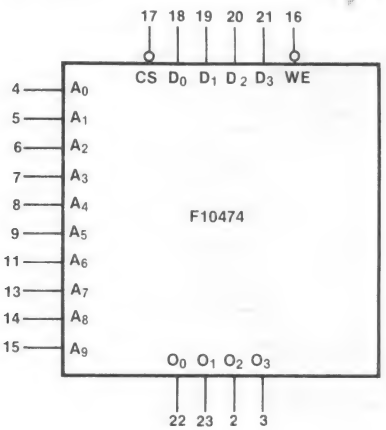
The F10474 is a 4096-bit read/write Random Access Memory (RAM), organized 1024 words by four bits per word. It is designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an active-LOW Chip Select line.

- **Address Access Time — 10 ns Max**
- **Chip Select Access Time — 5 ns Max**
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation — 0.29 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{CS}$	Chip Select Input (Active LOW)
A_0–A_9	Address Inputs
D_0–D_3	Data Inputs
O_0–O_3	Data Outputs

Logic Symbol

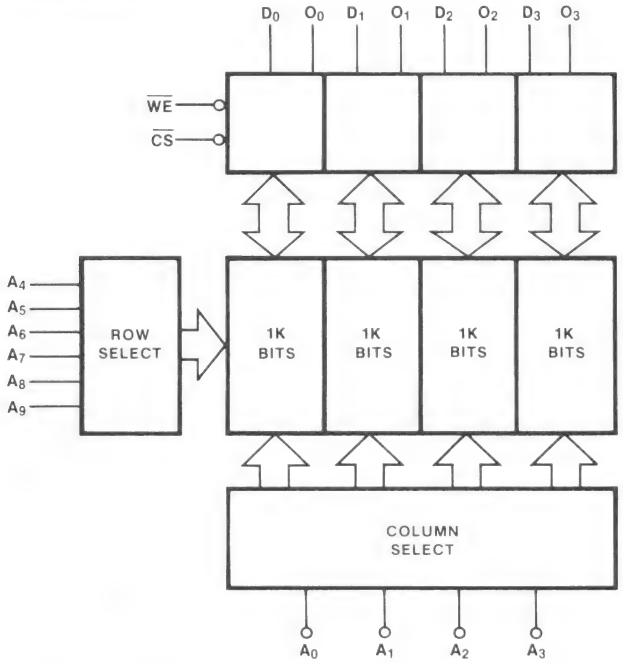


V_{CC} = Pin 24
V_{CCA} = Pin 1
V_{EE} = Pin 12
NC = Pin 10

Connection Diagram

24-Pin DIP (Top View)

Logic Diagram



Functional Description

The F10474 is a fully decoded 4096-bit read/write random access memory, organized 1024 words by four bits. Word selection is achieved by means of a 10-bit address, A_0 through A_9.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at D_0–D_3 is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the outputs (O_0–O_3).

The output of the F10474 is an unterminated emitter follower, which allows maximum flexibility in choosing connection configurations. In many applications such as memory expansion, the outputs of many F10474 devices can be tied together. In other applications the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is OFF.

Truth Table

Inputs			Outputs	
$\overline{CS}$	$\overline{WE}$	D_n	O_n	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Data	Read

H = HIGH Voltage Levels = −0.9 V (Nominal)
L = LOW Voltage Levels = −1.7 V (Nominal)
X = Don't Care
Data = Previously stored data

Notes

Notes

Notes

TTL Family Specifications

Absolute Maximum Ratings: Above which the useful life may be impaired

Storage Temperature	−65° to +150° C
Supply Voltage Range	−0.5 V to +7.0 V
Input Voltage (dc)[1][2]	−0.5 V to V_{CC} (RAMs)
	−1.5 V to V_{CC} (PROMs)
Voltage Applied to Outputs[2][3] (output HIGH)	−0.5 V to +5.5 V (RAMs)
	−1.5 V to +5.5 V (PROMs)
Lead Temperature (Soldering, 10 sec)	300° C
Maximum Junction Temperature (T_j)	+175° C
Output Current	+20 mA
Input Current (DC)	-12 mA to +5.0 mA

Guaranteed Operating Ranges

	Supply Voltage (V_{CC})	Case Temperature (T_C)	Maximum Low-Level Input Voltage (V_{IL})[8]	Minimum High-Level Input Voltage (V_{IH})[8]
Commercial	5.0 V ± 5%	0° C to +75° C	0.8V	2.1 V (RAMs) 2.0V (PROMs)
Military	5.0 V ± 10%	-55° C to +125° C		

Device Design Characteristics

Symbol	Characteristic	Typ	Unit	Condition
C_{IN}	Input Pin Capacitance	4.0	pF	Measured with a Pulse
C_{OUT}	Output Pin Capacitance	7.0	pF	Technique

DC, FN and AC performance characteristics and test conditions listed with each device (see note 8)

Notes
1. Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
2. These values may be exceeded as required during PROM programming.
3. Output current limit required.
4. Unless stated otherwise in individual device specification.
5. Functional testing done at input levels $V_{IL} = V_{OL\ Max}$ (0.45V), $V_{IH} = V_{OH\ Min}$ (2.4V)
6. PROM programmability verified through test row and test column.
7. PROM input levels on unprogrammed devices verified through testing of test row and test column.
8. Static condition only

All TTL RAM products in ceramic packages: dual-in-line, flatpak and leadless chip carrier are polyimide die-coated to decrease sensitivity to alpha particles emitted primarily by the seal glass and ceramic of the package.

FAIRCHILD
A Schlumberger Company

93415/93L415
1024 x 1-Bit Static Random Access Memory

Memory and High Speed Logic

Description

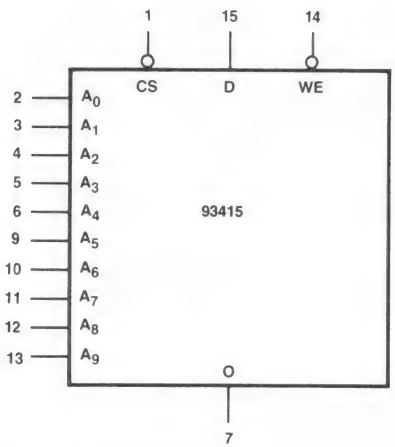
The 93415 is a 1024-bit read/write Random Access Memory (RAM), organized 1024 words by one bit. It is designed for high speed cache, control and buffer storage applications. The device includes full on-chip decoding, separate Data input and non-inverting Data output, as well as an active LOW Chip Select line.

- **Commercial Address Access Time**
  93415 — 25 to 60 ns Max
- **Military Address Access Time**
  93415 — 30 to 70 ns Max
- **Low Power Version Also Available (93L415)**
- **Features Open Collector Output**
- **Power Dissipation — 0.46 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{CS}$	Chip Select Input (Active LOW)
A_0–A_9	Address Inputs
$\overline{WE}$	Write Enable Input (Active LOW)
D	Data Input
O	Data Output

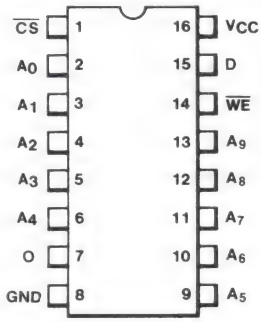
Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Connection Diagram

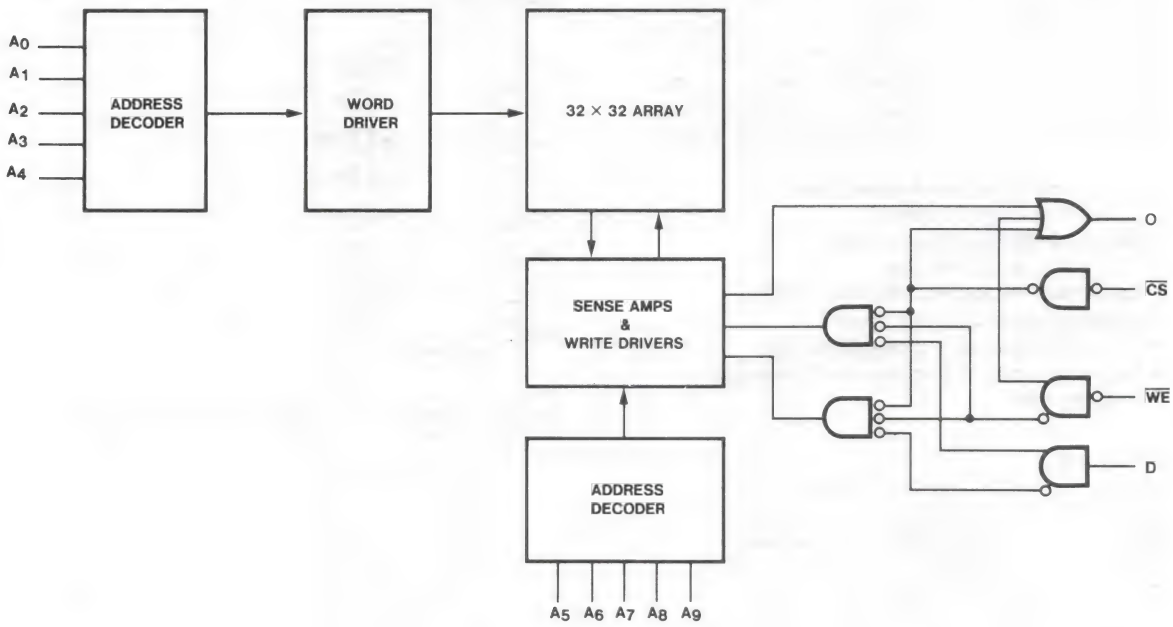
16-Pin DIP (Top View)



Note:
The 16-pin Flatpak version has the same pinout connections as the Dual In-line package.

4

Logic Diagram



Functional Description

The 93415 is a fully decoded 1024-bit read/write Random Access Memory organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A_0 through A_9.

One Chip Select input is provided for easy memory array expansion of up to 2048 bits without the need for external decoding. For larger memories, the fast chip select access time permits direct address decoding without an increase in overall memory access time.

The read and write functions of the 93415 are controlled by the state of the active LOW Write Enable ($\overline{WE}$) input. When $\overline{WE}$ is held LOW and the chip is selected, the data at D is written into the location specified by the binary address present at A_0 through A_9. Since the write function is level triggered, data must be held stable at the data input for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. When $\overline{WE}$ is held HIGH and the chip selected, data is read from the addressed location and presented at the output (O).

An open collector output is provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93415s can be tied together. In other applications the wired-OR is not used. In either case an external pull-up resistor of R_L value must be used to provide a HIGH at the output

when it is off. Any R_L value within the range specified below may be used.

$$\frac{V_{CC}\,(Max)}{I_{OL} - FO\,(1.6)} \leq R_L \leq \frac{V_{CC}\,(Min) - V_{OH}}{n\,(I_{CEX}) + FO\,(0.04)}$$

R_L is in kΩ
n = number of wired-OR outputs tied together
FO = number of TTL Unit Loads (UL) driven
I_{CEX} = Memory Output Leakage Current
V_{OH} = Required Output HIGH Level at Output Node
I_{OL} = Output LOW Current

The minimum R_L value is limited by the output current sinking ability. The maximum R_L value is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}.
One Unit Load = 40 μA HIGH/1.6 mA LOW.
FO_{MAX} = 5 UL.

Truth Table

Inputs			Output	
$\overline{CS}$	$\overline{WE}$	D	O	Mode
H	X	X	H	Not Selected
L	L	L	H	Write "0"
L	L	H	H	Write "1"
L	H	X	D_{OUT}	Read

H = HIGH Voltage Level (2.4 V)
L = LOW Voltage Level (.5 V)
X = Don't Care (HIGH or LOW)

DC Characteristics: Over operating temperature ranges (Note 1)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{OL}	Output LOW Voltage		0.3	0.45	V	V_{CC} = Min, I_{OL} = 16 mA
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for All Inputs[5]
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for All Inputs[5]
I_{IL}	Input LOW Current		−250	−400[7]	μA	V_{CC} = Max, V_{IN} = 0.4 V
I_{IH}	Input HIGH Current		1.0	40	μA	V_{CC} = Max, V_{IN} = 4.5 V
I_{IHB}	Input Breakdown Current			1.0	mA	V_{CC} = Max, V_{IN} = V_{CC}
V_{IC}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = Max, I_{IN} = −10 mA
I_{CEX}	Output Leakage Current		1.0	100	μA	V_{CC} = Max, V_{OUT} = 4.5 V
I_{CC}	Power Supply Current			65	mA	93L415-35, 93L415-45, 93L415-60 (commercial)
				75	mA	93L415-40, 93L415-50, 93L415-70 (military)
				125	mA	93415-25, 93415-30 (commercial)
				135	mA	93415-30, 93415-40 (military)
				155	mA	93415A, 93415-45 (commercial)
				170	mA	93415-60 (military)
						V_{CC} = Max, Note 6

Notes
1. Typical values are at V_{CC} = 5.0 V. T_C = +25° C and maximum loading.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
3. Short circuit to ground not to exceed one second.
4. t_W measured at t_{WSA} = Min, t_{WSA} measured at t_W = Min.
5. Tested under static condition only.
6. All inputs GND
   Output open
7. I_{IL} = −300 μA for 93L415

Commercial

AC Performance Characteristics: $V_{CC} = 5.0 \pm 5\%$, GND = 0 V, T_C = 0° C to +75° C

Symbol	Characteristic	93415-25		93415-30 93415A		93415-45		Unit	Condition
		Min	Max	Min	Max	Min	Max		
	Read Timing								
t_{ACS}	Chip Select Access Time		15		20		35	ns	*Figures 3a, 3b*
t_{RCS}	Chip Select Recovery Time		20		20		35	ns	
t_{AA}	Address Access Time[2]		25		30		45	ns	
	Write Timing								
t_W	Write Pulse Width to Guarantee Writing[4]	15		20		35		ns	*Figure 4*
t_{WSD}	Data Setup Time Prior to Write	5		5		5		ns	
t_{WHD}	Data Hold Time after Write	5		5		5		ns	
t_{WSA}	Address Setup Time Prior to Write[4]	5		5		5		ns	
t_{WHA}	Address Hold Time after Write	5		5		5		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		5		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		5		ns	
t_{WS}	Write Enable to Output Disable		15		20		35	ns	
t_{WR}	Write Recovery Time		15		20		40	ns	
t_{WR}	Write Recovery Time (93415A)				25			ns	

Military

AC Performance Characteristics: $V_{CC} = 5.0$ V $\pm$ 10%, GND = 0 V, T_C = -55° C to +125° C

Symbol	Characteristic	93415-30		93415-40		93415-60		Unit	Condition
		Min	Max	Min	Max	Min	Max		
	Read Timing								
t_{ACS}	Chip Select Access Time		20		25		45	ns	*Figures 3a, 3b*
t_{RCS}	Chip Select Recovery Time		20		25		50	ns	
t_{AA}	Address Access Time[2]		30		40		60	ns	
	Write Timing								
t_W	Write Pulse Width to Guarantee Writing[4]	20		25		40		ns	*Figure 4*
t_{WSD}	Data Setup Time Prior to Write	5		5		5		ns	
t_{WHD}	Data Hold Time after Write	5		5		5		ns	
t_{WSA}	Address Setup Time Prior to Write[4]	5		10		15		ns	
t_{WHA}	Address Hold Time after Write	5		5		5		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		5		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		5		ns	
t_{WS}	Write Enable to Output Disable		20		25		45	ns	
t_{WR}	Write Recovery Time		20		25		50	ns	

Notes on page 4-7

Commercial

AC Performance Characteristics: $V_{CC} = 5.0 \pm 5\%$, GND = 0 V, T_C = 0° C to +75° C

Symbol	Characteristic	93L415-35		93L415-45		93L415-60		Unit	Condition
		Min	Max	Min	Max	Min	Max		
	Read Timing								
t_{ACS}	Chip Select Access Time		25		30		40	ns	*Figures 3a, 3b*
t_{RCS}	Chip Select Recovery Time		25		30		40	ns	
t_{AA}	Address Access Time[2]		35		45		60	ns	
	Write Timing								
t_W	Write Pulse Width to Guarantee Writing[4]	30		35		45		ns	*Figure 4*
t_{WSD}	Data Setup Time Prior to Write	5		5		5		ns	
t_{WHD}	Data Hold Time after Write	5		5		5		ns	
t_{WSA}	Address Setup Time Prior to Write[4]	5		5		10		ns	
t_{WHA}	Address Hold Time after Write	5		5		5		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		5		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		5		ns	
t_{WS}	Write Enable to Output Disable		20		25		45	ns	
t_{WR}	Write Recovery Time		30		35		45	ns	

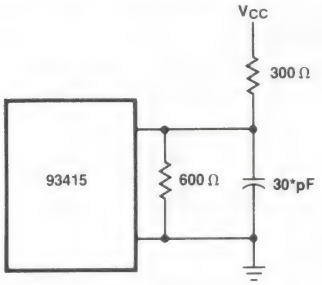
Military

AC Performance Characteristics: $V_{CC} = 5.0\ V \pm 10\%$, GND = 0 V, T_C = -55° C to +125° C

Symbol	Characteristic	93L415-40		93L415-50		93L415-70		Unit	Condition
		Min	Max	Min	Max	Min	Max		
	Read Timing								
t_{ACS}	Chip Select Access Time		30		35		45	ns	*Figures 3a, 3b*
t_{RCS}	Chip Select Recovery Time		25		30		50	ns	
t_{AA}	Address Access Time[2]		40		50		70	ns	
	Write Timing								
t_W	Write Pulse Width to Guarantee Writing[4]	35		40		50		ns	*Figure 4*
t_{WSD}	Data Setup Time Prior to Write	5		5		10		ns	
t_{WHD}	Data Hold Time after Write	5		5		10		ns	
t_{WSA}	Address Setup Time Prior to Write[4]	10		10		10		ns	
t_{WHA}	Address Hold Time after Write	5		5		10		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		10		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		10		ns	
t_{WS}	Write Enable to Output Disable		25		30		45	ns	
t_{WR}	Write Recovery Time		30		40		55	ns	

Notes on preceding page

Fig. 1 AC Test Circuit



*Includes jig and probe capacitance

Fig. 2 AC Test Input Levels

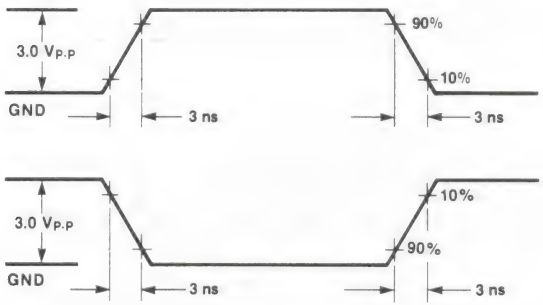
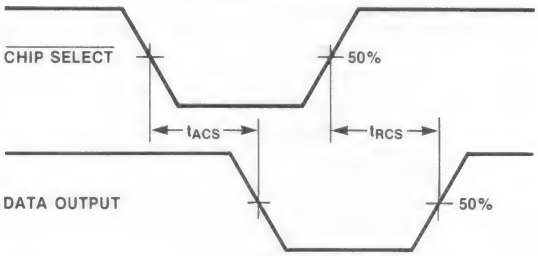


Fig. 3 Read Mode Timing

3a Read Mode Propagation Delay from Chip Select



3b Read Mode Propagation Delay from Address

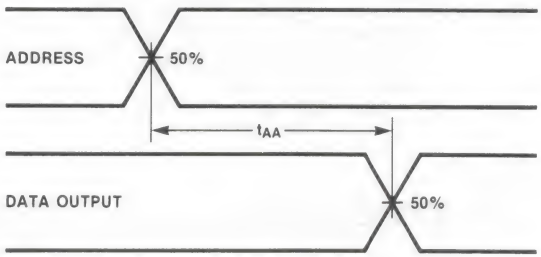
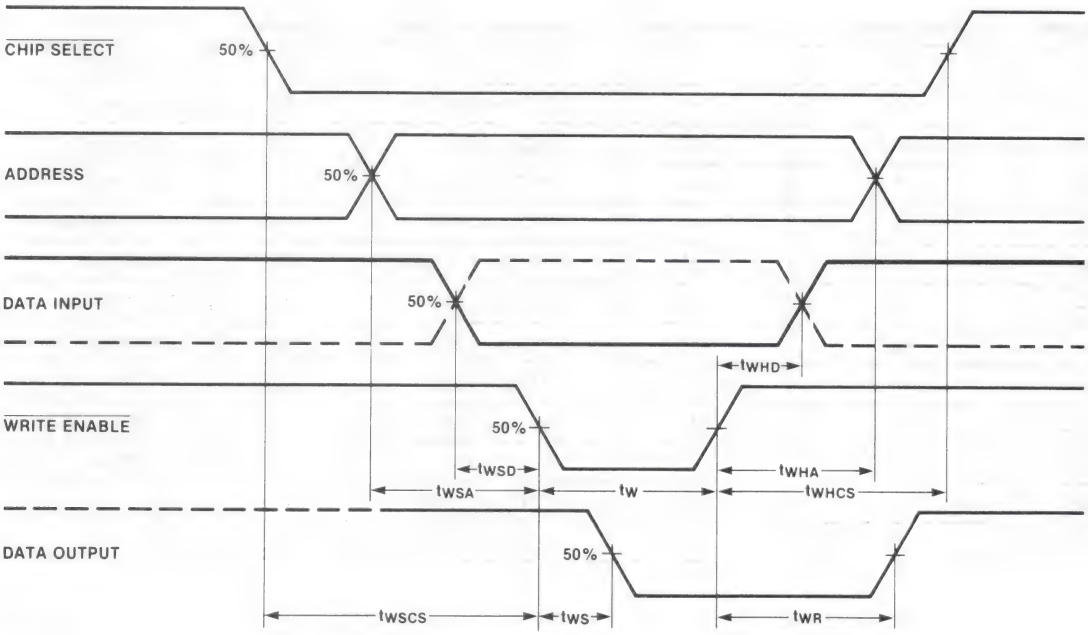


Fig. 4 Write Mode Timing



Notes

1. Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.
2. Input voltage levels for worst case AC test are 3.0/0.0 V.

Ordering Information

Part Number	Access Time (ns)	Power (mA)	Temperature Range	Package	Order Code
93415-25	25	125	0° C to +75° C	XX	93415XX25
93415A	30	155	0° C to +75° C	XX	93415AXX
93415-30	30	125	0° C to +75° C	XX	93415XX30
93415-30	30	135	−55° C to +125° C	YY	93415YY30
93L415-35	35	65	0° C to +75° C	XX	93L415XX35
93415-40	40	135	−55° C to +125° C	YY	93415YY40
93L415-40	40	75	−55° C to +125° C	YY	93L415YY40
93415-45	45	155	0° C to +75° C	XX	93415XX
93L415-45	45	65	0° C to +75° C	XX	93L415XX45
93L415-50	50	75	−55° C to +125° C	YY	93L415YY50
93L415-60	60	65	0° C to +75° C	XX	93L415XX
93415-60	60	170	−55° C to +125° C	YY	93415YY
93L415-70	70	75	−55° C to +125° C	YY	93L415YY

Packages and Optional Processing (See Section 9)

XX — Commercial

Without Optional Processing	With Optional Processing
DC	DCQR — Ceramic Dip
FC	FCQR — Cerpak
PC	PCQR — Plastic Dip

YY — Military

Without Optional Processing	With Optional Processing
DM	DMQB — Ceramic Dip
FM	FMQB — Cerpak

Optional Processing

QB = Mil Std 883
Method 5004 and 5005, Level B
QR = Commercial Device with
160 Hour Burn in or Equivalent

Note:
Because every combination of packaging, speed, temperature, and optional processing is not in stock, availability of some combinations is not on an immediate basis.

FAIRCHILD
A Schlumberger Company

93422
256 x 4-Bit Static Random Access Memory

Memory and High Speed Logic

Description

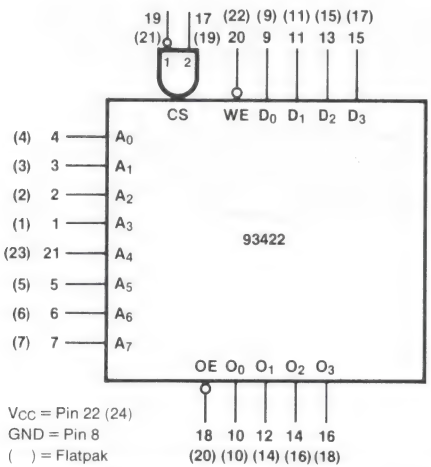
The 93422 is a 1024-bit read/write Random Access Memory (RAM), organized 256 words by four bits. It is designed for high speed cache, control and buffer storage applications. The 93422 is available in two speeds, "standard" speed and an "A" grade. The device includes full on-chip decoding, separate Data inputs and non-inverting Data outputs, as well as two Chip Select lines.

- **Commercial Address Access Time**
  - **93422 — 45 ns Max**
  - **93422A — 35 ns Max**
- **Military Address Access Time**
  - **93422 — 60 ns Max**
  - **93422A — 45 ns Max**
- **Fully TTL Compatible**
- **Features Three State Outputs**
- **Power Dissipation — 0.46 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

A_0–A_7	Address Inputs
D_0–D_3	Data Inputs
$\overline{CS}_1$	Chip Select Input (Active LOW)
CS_2	Chip Select Input (Active HIGH)
$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{OE}$	Output Enable Input (Active LOW)
O_0–O_3	Data Outputs

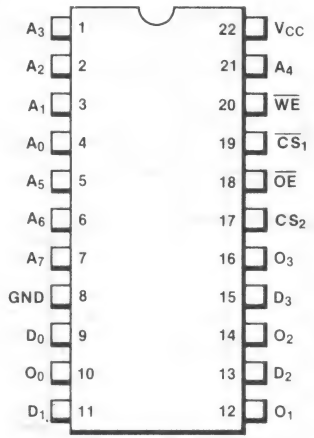
Logic Symbol



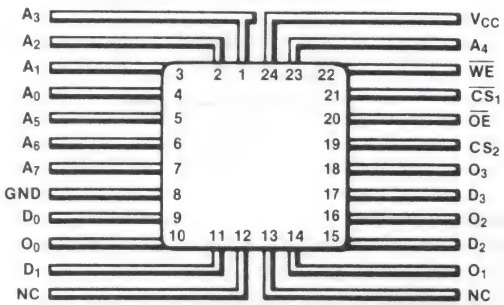
VCC = Pin 22 (24)
GND = Pin 8
( ) = Flatpak

Connection Diagrams

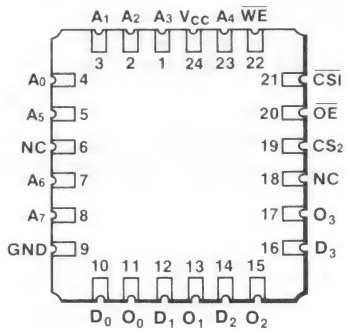
22-Pin DIP (Top View)



24-Pin Flatpak (Top View)



24-Pin Leadless Chip Carrier (Top View)



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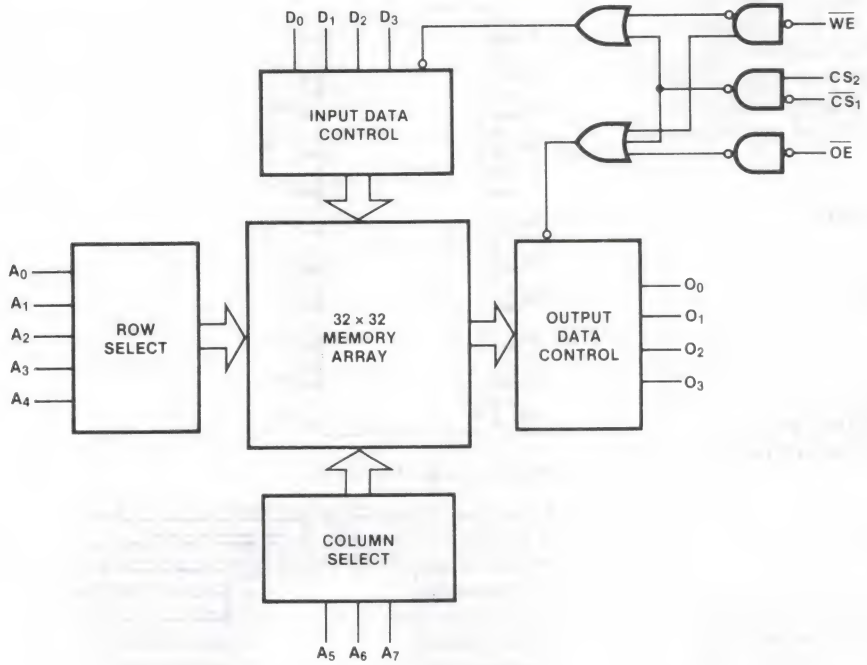
Logic Diagram



Functional Description

The 93422 is a fully decoded 1024-bit Random Access Memory organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, A_0 through A_7.

Two Chip Select inputs, inverting and non-inverting, are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of the chip selects from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$) input. When $\overline{WE}$ is held LOW and the chip is selected, the data at D_0–D_3 is written into the addressed location. Since the write function is level-triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the outputs (O_0–O_3).

The 93422 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled. This allows optimization of word expansion in bus organized systems.

Truth Table

Inputs				Outputs	
$\overline{OE}$	$\overline{CS_1}$	CS_2	$\overline{WE}$	3-State	Mode
X	H	X	X	HIGH Z	Not Selected
X	X	L	X	HIGH Z	Not Selected
L	L	H	H	D_{OUT}	READ
X	L	H	L	HIGH Z	WRITE
H	X	X	X	HIGH Z	Output Disabled

H = HIGH Voltage Level (2.4 V)
L = LOW Voltage Level (.5 V)
X = Don't Care (HIGH or LOW)
High Z = High-Impedance

DC Performance Characteristics: Over operating temperature ranges (Note 1)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition	
V_{OL}	Output LOW Voltage		0.3	0.45	V	V_{CC} = Min, I_{OL} = 8 mA	
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for All Inputs [5]	
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for All Inputs [5]	
V_{OH}	Output HIGH Voltage	2.4			V	V_{CC} = Min, I_{OH} = −5.2 mA	
I_{IL}	Input LOW Current		−150	−300	μA	V_{CC} = Max, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current		1.0	40	μA	V_{CC} = Max, V_{IN} = 4.5 V	
I_{IHB}	Input Breakdown Current			1.0	mA	V_{CC} = Max, V_{IN} = V_{CC}	
V_{IC}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = Max, I_{IN} = −10 mA	
I_{OZH} I_{OZL}	Output Current (HIGH Z)			50 −50	μA	V_{CC} = Max, V_{OUT} = 2.4 V V_{CC} = Max, V_{OUT} = 0.5 V	
I_{OS}	Output Current Short Circuit to Ground	−10		−70	mA	V_{CC} = Max, Note 3	
I_{CC}	Power Supply Current			120 130	mA	Commercial Military	V_{CC} = Max All Inputs GND All Outputs Open

Notes
1. Typical values are at V_{CC} = 5.0 V. T_C = +25° C and maximum loading.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
3. Short circuit to ground not to exceed one second.
4. t_W measured at t_{WSA} = Min. t_{WSA} measured at t_W = Min.
5. Static condition only.

Commercial
AC Performance Characteristics: $V_{CC} = 5.0\ V \pm 5\%$, GND = 0 V, $T_C = 0°C$ to $+75°C$

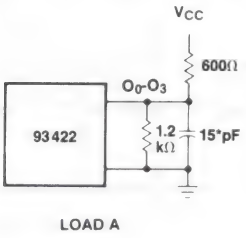
Symbol	Characteristic	A Min	A Max	Std Min	Std Max	Unit	Condition
	Read Timing						
t_{ACS}	Chip Select Access Time		30		30	ns	
t_{ZRCS}	Chip Select to HIGH Z		30		30	ns	
t_{AOS}	Output Enable Access Time		30		30	ns	*Figures 3a, 3b, 3c*
t_{ZROS}	Output Enable to HIGH Z		30		30	ns	
t_{AA}	Address Access Time[2]		35		45	ns	
	Write Timing						
t_W	Write Pulse Width to Guarantee Writing[4]	25		30		ns	
t_{WSD}	Data Setup Time Prior to Write	5		5		ns	
t_{WHD}	Data Hold Time after Write	5		5		ns	
t_{WSA}	Address Setup Time Prior to Write[4]	5		5		ns	*Figure 4*
t_{WHA}	Address Hold Time after Write	5		5		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		ns	
t_{ZWS}	Write Enable to HIGH Z		35		35	ns	
t_{WR}	Write Recovery Time		35		40	ns	

Military
AC Performance Characteristics: $V_{CC} = 5.0\ V \pm 10\%$, GND = 0 V, $T_C = -55°C$ to $+125°C$

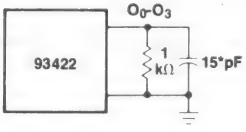
Symbol	Characteristic	A Min	A Max	Std Min	Std Max	Unit	Condition
	Read Timing						
t_{ACS}	Chip Select Access Time		35		45	ns	
t_{ZRCS}	Chip Select to HIGH Z		35		45	ns	
t_{AOS}	Output Enable Access Time		35		45	ns	*Figures 3a, 3b, 3c*
t_{ZROS}	Output Enable to HIGH Z		35		45	ns	
t_{AA}	Address Access Time[2]		45		60	ns	
	Write Timing						
t_W	Write Pulse Width to Guarantee Writing[4]	35		40		ns	
t_{WSD}	Data Setup Time Prior to Write	5		5		ns	
t_{WHD}	Data Hold Time after Write	5		5		ns	
t_{WSA}	Address Setup Time Prior to Write[4]	5		5		ns	*Figure 4*
t_{WHA}	Address Hold Time after Write	5		5		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		ns	
t_{ZWS}	Write Enable to HIGH Z		40		45	ns	
t_{WR}	Write Recovery Time		40		50	ns	

Notes on preceding page

Fig. 1 AC Test Output Load



LOAD A



LOAD B

*Includes jig and probe capacitance

Note: Load A is used for all production testing.

Fig. 2 AC Test Input Levels

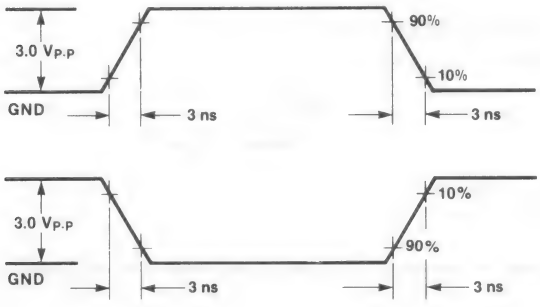
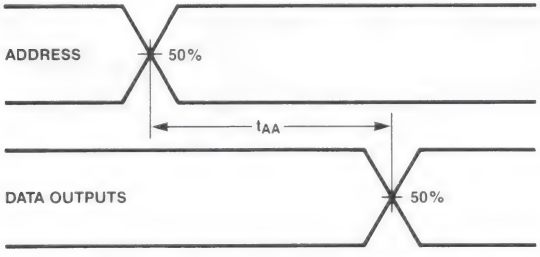
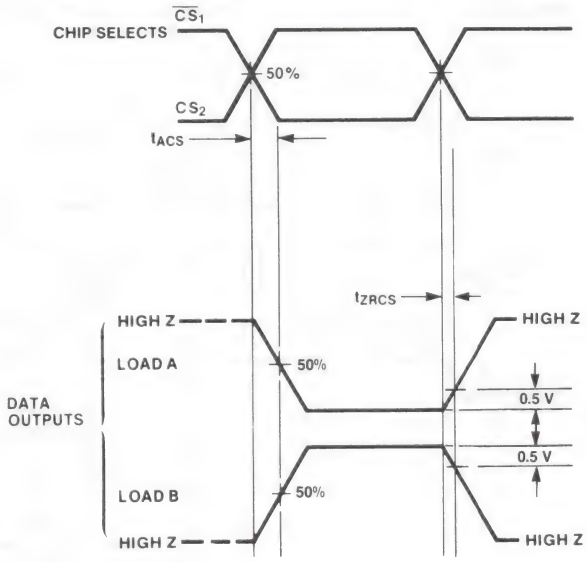


Fig. 3 Read Mode Timing

a Read Mode Propagation Delay from Address



3b Read Mode Propagation Delay from Chip Select



3c Read Mode Propagation Delay from Output Enable

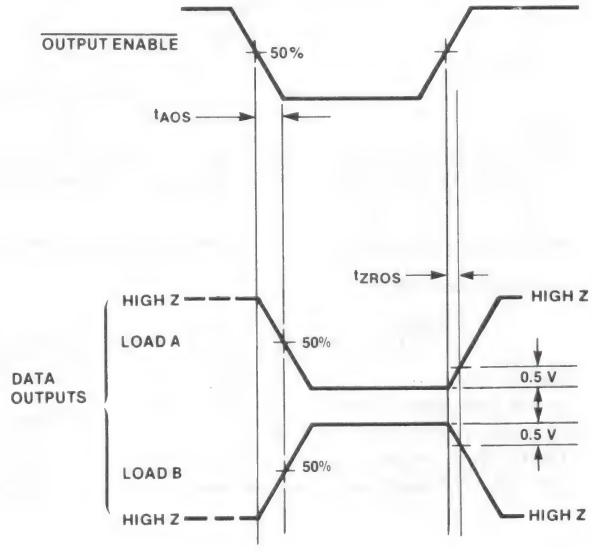


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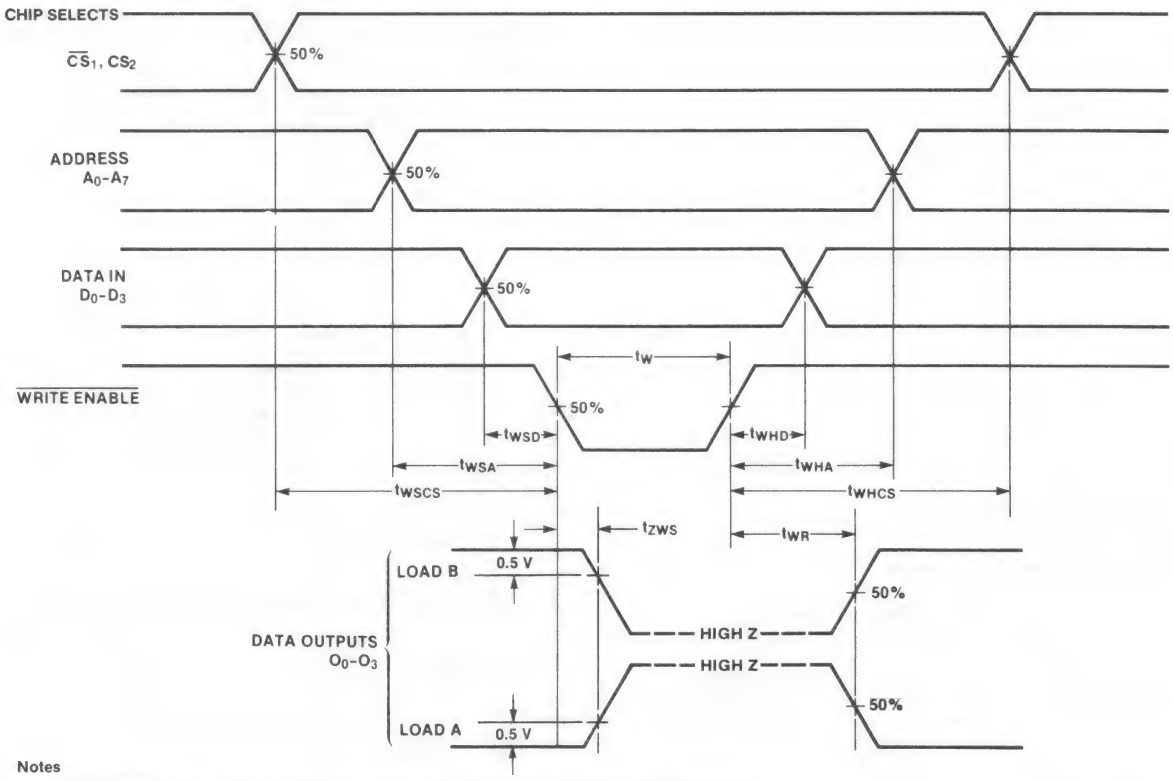
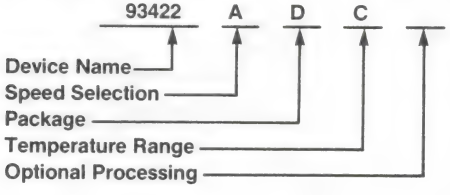
Fig. 4 Write Mode Timing



Notes

1. Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.
2. Input voltage levels for worst case AC test are 3.0/0.0 V.

Ordering Information



Speed Selection
Blank = Standard Speed
A = 'A' Grade

Packages and Outlines (See Section 9)
D = Ceramic DIP
F = Flatpak
L = Leadless Chip Carrier
P = Plastic DIP

Temperature Range
C = 0°C to +75°C
M = −55°C to +125°C

Optional Processing
QB = Mil Std 883
Method 5004 and 5005, Level B
QR = Commercial Device with
160 Hour Burn In or Equivalent

FAIRCHILD
A Schlumberger Company

93L422
256 x 4-Bit Static Random Access Memory

Memory and High Speed Logic

Description

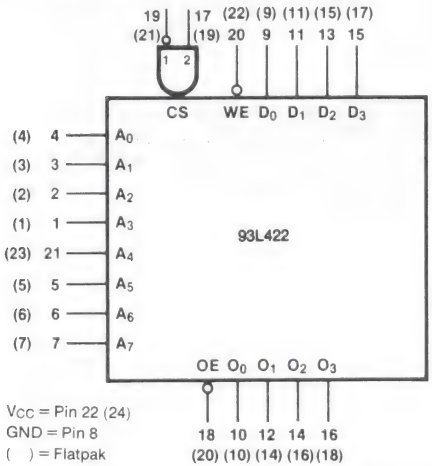
The 93L422 is a 1024-bit read/write Random Access Memory (RAM), organized 256 words by four bits. It is designed for high speed cache, control and buffer storage applications. The 93L422 is available in two speeds, "standard" speed and an "A" grade. The device includes full on-chip decoding, separate Data inputs and non-inverting Data outputs, as well as two Chip Select lines.

- **Commercial Address Access Time**
  - **93L422 — 60 ns Max**
  - **93L422A — 45 ns Max**
- **Military Address Access Time**
  - **93L422 — 75 ns Max**
  - **93L422A — 55 ns Max**
- **Fully TTL Compatible**
- **Features Three State Outputs**
- **Power Dissipation — 0.25 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

A_0–A_7	Address Inputs
D_0–D_3	Data Inputs
$\overline{CS}_1$	Chip Select Input (Active LOW)
CS_2	Chip Select Input (Active HIGH)
$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{OE}$	Output Enable Input (Active LOW)
O_0–O_3	Data Outputs

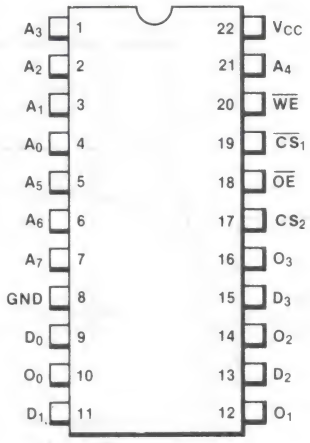
Logic Symbol



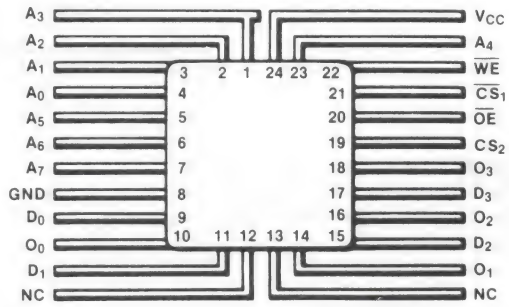
VCC = Pin 22 (24)
GND = Pin 8
( ) = Flatpak

Connection Diagrams

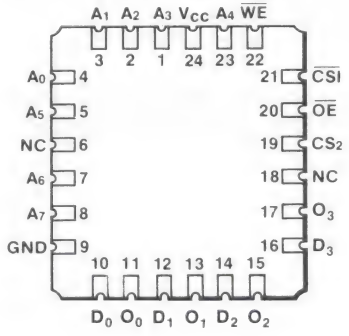
22-Pin DIP (Top View)



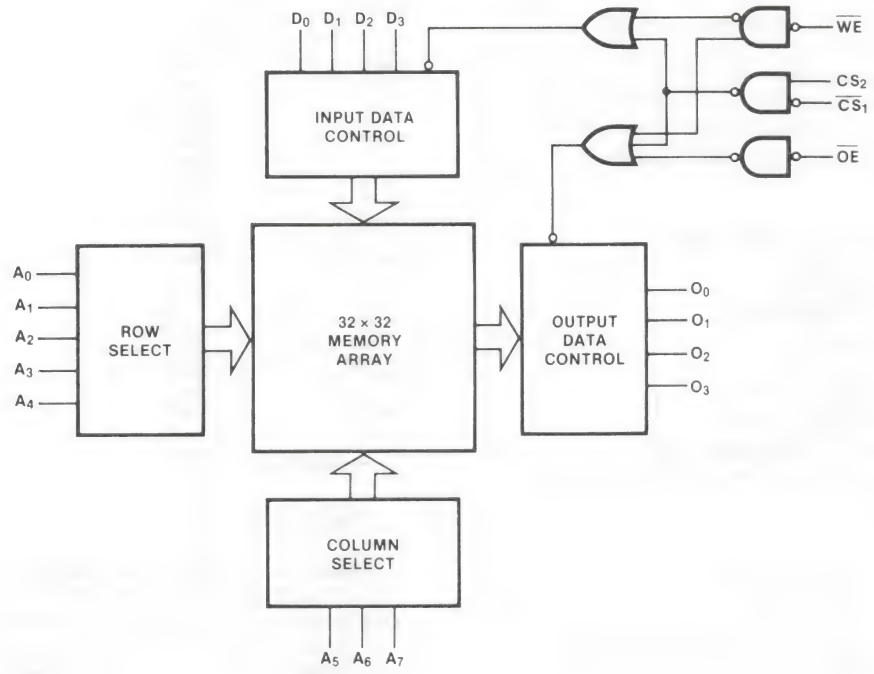
24-Pin Flatpak (Top View)



24-Pin Leadless Chip Carrier (Top View)



Logic Diagram



Functional Description

The 93L422 is a fully decoded 1024-bit Random Access Memory organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, A_0 through A_7.

Two Chip Select inputs, inverting and non-inverting, are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of the chip selects from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$) input. When $\overline{WE}$ is held LOW and the chip is selected, the data at D_0–D_3 is written into the addressed location. Since the write function is level-triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the outputs (O_0–O_3).

The 93L422 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled. This allows optimization of word expansion in bus organized systems.

Truth Table

Inputs				Outputs	
$\overline{OE}$	$\overline{CS_1}$	CS_2	$\overline{WE}$	3-State	Mode
X	H	X	X	HIGH Z	Not Selected
X	X	L	X	HIGH Z	Not Selected
L	L	H	H	D_{OUT}	READ
X	L	H	L	HIGH Z	WRITE
H	X	X	X	HIGH Z	Output Disabled

H = HIGH Voltage Level (2.4 V)
L = LOW Voltage Level (.5 V)
X = Don't Care (HIGH or LOW)
High Z = High-Impedance

DC Performance Characteristics: Over operating temperature ranges (Note 1)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition	
V_{OL}	Output LOW Voltage		0.3	0.45	V	V_{CC} = Min, I_{OL} = 8 mA	
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for All Inputs [5]	
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for All Inputs [5]	
V_{OH}	Output HIGH Voltage	2.4			V	V_{CC} = Min, I_{OH} = −5.2 mA	
I_{IL}	Input LOW Current		−150	−300	μA	V_{CC} = Max, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current		1.0	40	μA	V_{CC} = Max, V_{IN} = 4.5 V	
I_{IHB}	Input Breakdown Current			1.0	mA	V_{CC} = Max, V_{IN} = V_{CC}	
V_{IC}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = Max, I_{IN} = −10 mA	
I_{OZH} I_{OZL}	Output Current (HIGH Z)			50 −50	μA	V_{CC} = Max, V_{OUT} = 2.4 V V_{CC} = Max, V_{OUT} = 0.5 V	
I_{OS}	Output Current Short Circuit to Ground	−10		−70	mA	V_{CC} = Max, Note 3	
I_{CC}	Power Supply Current			80 90	mA	Commercial Military	V_{CC} = Max All Inputs GND All Outputs Open

Notes
1. Typical values are at V_{CC} = 5.0 V, T_C = +25° C and maximum loading.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
3. Short circuit to ground not to exceed one second.
4. t_W measured at t_{WSA} = Min. t_{WSA} measured at t_W = Min.
5. Static condition only.

Commercial

AC Performance Characteristics: $V_{CC} = 5.0\ V \pm 5\%$, GND = 0 V, $T_C = 0°C$ to $+75°C$

Symbol	Characteristic	A Min	A Max	Std Min	Std Max	Unit	Condition
	Read Timing						
t_{ACS}	Chip Select Access Time		30		35	ns	
t_{ZRCS}	Chip Select to HIGH Z		30		35	ns	
t_{AOS}	Output Enable Access Time		30		35	ns	*Figures 3a, 3b, 3c*
t_{ZROS}	Output Enable to HIGH Z		30		35	ns	
t_{AA}	Address Access Time[2]		45		60	ns	
	Write Timing						
t_W	Write Pulse Width to Guarantee Writing[4]	30		45		ns	
t_{WSD}	Data Setup Time Prior to Write	5		5		ns	
t_{WHD}	Data Hold Time after Write	5		5		ns	
t_{WSA}	Address Setup Time Prior to Write[4]	5		5		ns	*Figure 4*
t_{WHA}	Address Hold Time after Write	5		5		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		ns	
t_{ZWS}	Write Enable to HIGH Z		35		40	ns	
t_{WR}	Write Recovery Time		40		45	ns	

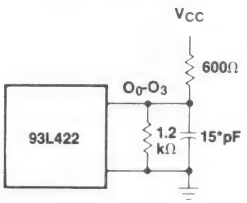
Military

AC Performance Characteristics: $V_{CC} = 5.0\ V \pm 10\%$, GND = 0 V, $T_C = -55°C$ to $+125°C$

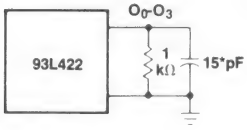
Symbol	Characteristic	A Min	A Max	Std Min	Std Max	Unit	Condition
	Read Timing						
t_{ACS}	Chip Select Access Time		40		45	ns	
t_{ZRCS}	Chip Select to HIGH Z		40		45	ns	
t_{AOS}	Output Enable Access Time		40		45	ns	*Figures 3a, 3b, 3c*
t_{ZROS}	Output Enable to HIGH Z		40		45	ns	
t_{AA}	Address Access Time[2]		55		75	ns	
	Write Timing						
t_W	Write Pulse Width to Guarantee Writing[4]	40		55		ns	
t_{WSD}	Data Setup Time Prior to Write	5		5		ns	
t_{WHD}	Data Hold Time after Write	5		5		ns	
t_{WSA}	Address Setup Time Prior to Write[4]	5		5		ns	*Figure 4*
t_{WHA}	Address Hold Time after Write	5		5		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		ns	
t_{ZWS}	Write Enable to HIGH Z		45		45	ns	
t_{WR}	Write Recovery Time		50		50	ns	

Notes on preceding page

Fig. 1 AC Test Output Load



LOAD A



LOAD B

*Includes jig and probe capacitance

Note: Load A is used for all production testing.

Fig. 2 AC Test Input Levels

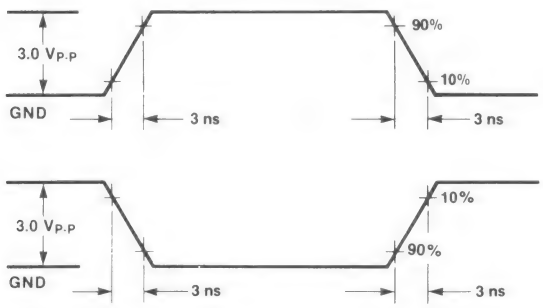
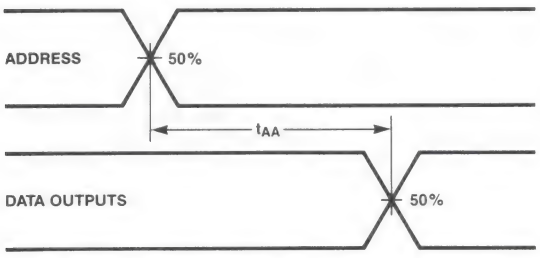
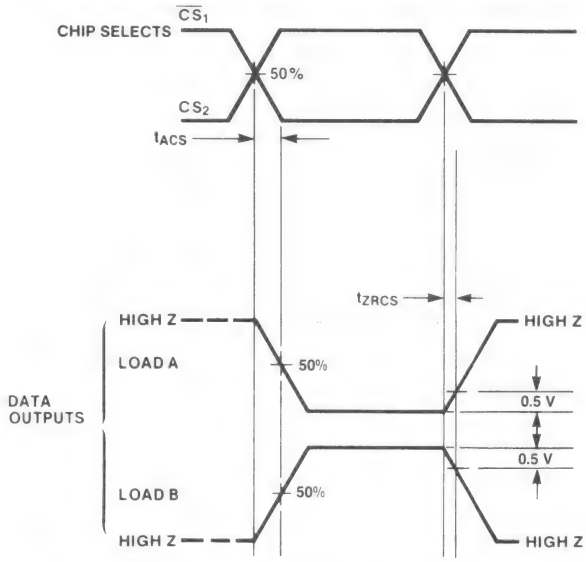


Fig. 3 Read Mode Timing

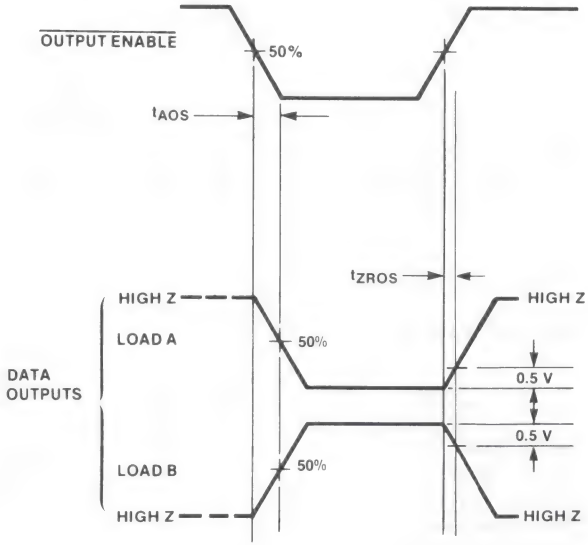
3a Read Mode Propagation Delay from Address



3b Read Mode Propagation Delay from Chip Select

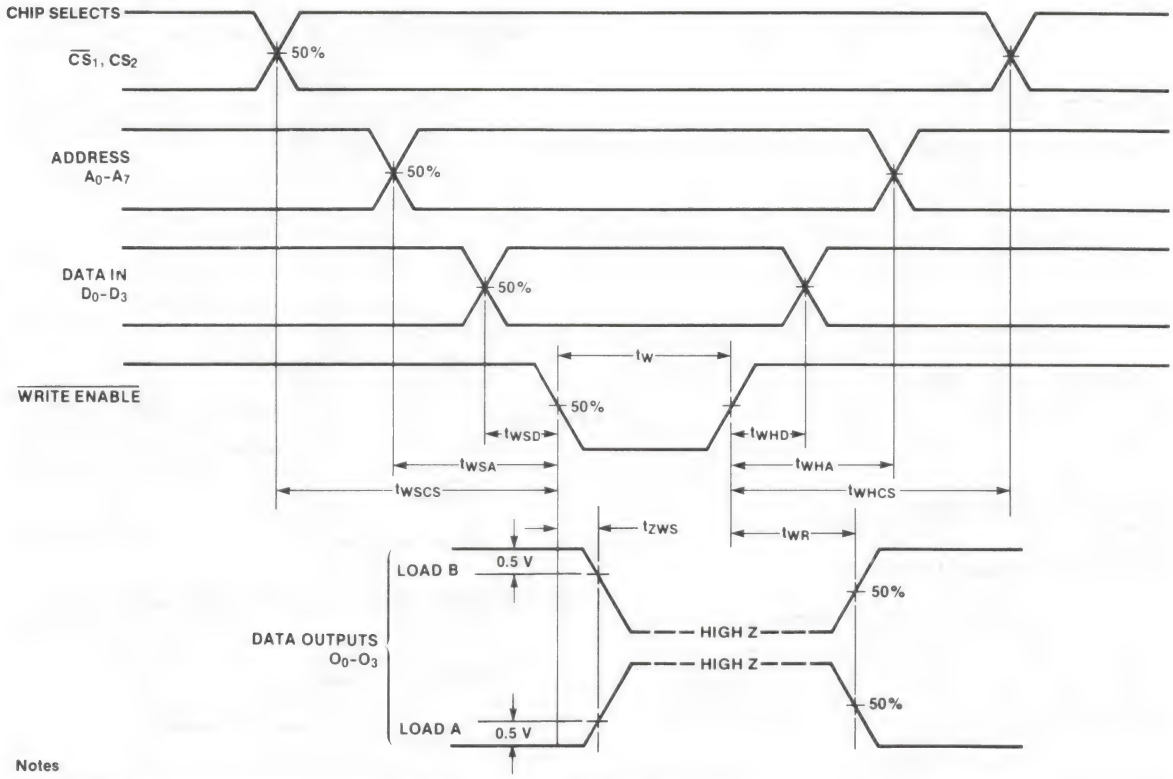


3c Read Mode Propagation Delay from Output Enable



4

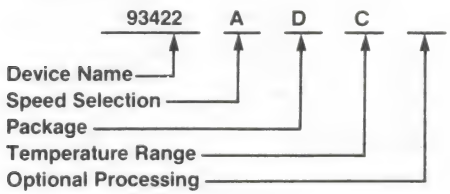
Fig. 4 Write Mode Timing



Notes

1. Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.
2. Input voltage levels for worst case AC test are 3.0/0.0 V.

Ordering Information



Speed Selection
Blank = Standard Speed
A = 'A' Grade

Packages and Outlines (See Section 9)
D = Ceramic DIP
F = Flatpak
L = Leadless Chip Carrier
P = Plastic DIP

Temperature Range
C = 0°C to +75°C
M = −55°C to +125°C

Optional Processing
QB = Mil Std 883
Method 5004 and 5005, Level B
QR = Commercial Device with
160 Hour Burn In or Equivalent

FAIRCHILD
A Schlumberger Company

93425/93L425
1024 x 1-Bit Static Random Access Memory

Memory and High Speed Logic

Description

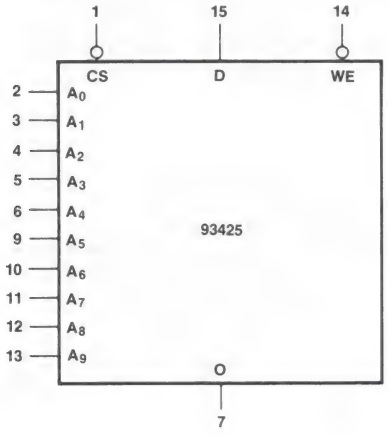
The 93425 is a 1024-bit read/write Random Access Memory (RAM), organized 1024 words by one bit. It is designed for high speed cache, control and buffer storage applications. The device includes full on-chip decoding, separate Data input and non-inverting Data output, as well as an active LOW Chip Select line.

- **Commercial Address Access Time**
  953425 — 20 to 60 ns Max
- **Military Address Access Time**
  93425 — 30 to 70 ns Max
- **Low Power Version Also Available (93L425)**
- **Features Three State Output**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{CS}$	Chip Select (Active LOW)
A_0–A_9	Address Inputs
$\overline{WE}$	Write Enable (Active LOW)
D	Data Input
O	Data Output

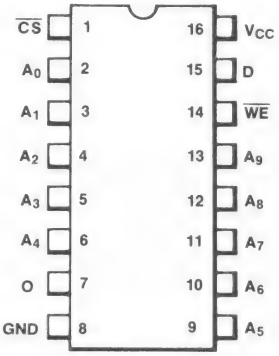
Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Connection Diagram

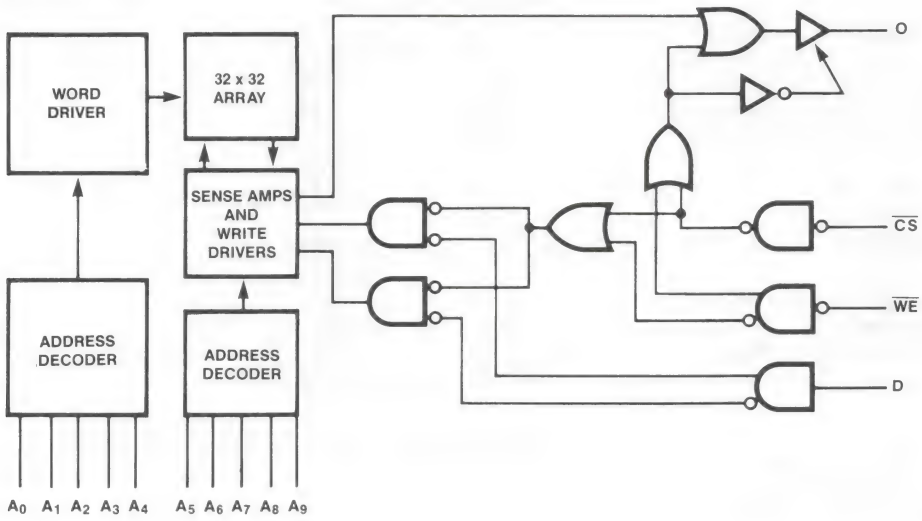
16-Pin DIP (Top View)



Note:
The 16 pin Flatpak version has the same pinout connections as the Dual In-line package.

4

Logic Diagram



Functional Description

The 93425 is a fully decoded 1024-bit read/write Random Access Memory organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A_0 through A_9.

One Chip Select input is provided for easy memory array expansion of up to 2048 bits without the need for external decoding. For larger memories, the fast chip select access time permits direct address decoding without an increase in overall memory access time.

The read and write functions of the 93425 are controlled by the state of the active LOW Write Enable ($\overline{WE}$) input. When $\overline{WE}$ is held LOW and the chip is selected, the data at D is written into the location specified by the binary address present at A_0 through A_9. Since the write function is level triggered, data must be held stable at the data input for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. When $\overline{WE}$ is held HIGH and the chip selected, data is read from the addressed location and presented at the output (O).

The 93425 has a three-state output which provides an active pull-up or pull-down when enabled and a high impedance (HIGH Z) state when disabled. The active pull-up provides drive capability for high capacitive loads while the high impedance state allows optimization of word expansion in bus organized systems.

Truth Table

Inputs			Output	
$\overline{CS}$	$\overline{WE}$	D	O	Mode
H	X	X	HIGH Z	Not Selected
L	L	L	HIGH Z	Write "0"
L	L	H	HIGH Z	Write "1"
L	H	X	D_{OUT}	Read

H = HIGH Voltage Level (2.4 V)
L = LOW Voltage Level (.5 V)
X = Don't Care (HIGH or LOW)

DC Performance Characteristics: Over operating temperature ranges (Note 1)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{OL}	Output LOW Voltage		0.3	0.45	V	V_{CC} = Min, I_{OL} = 16 mA
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for All Inputs[5]
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for All Inputs[5]
V_{OH}	Output HIGH Voltage	2.4			V	V_{CC} = Min, I_{OH} = −5.2 mA
I_{IL}	Input LOW Current		−250	−400[7]	μA	V_{CC} = Max, V_{IN} = 0.4 V
I_{IH}	Input HIGH Current		1.0	40	μA	V_{CC} = Max, V_{IN} = 4.5 V
I_{IHB}	Input Breakdown Current			1.0	mA	V_{CC} = Max, V_{IN} = V_{CC}
V_{IC}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = Max, I_{IN} = −10 mA
I_{OZH} I_{OZL}	Output Current (HIGH Z)			50 −50	μA	V_{CC} = Max, V_{OUT} = 2.4 V V_{CC} = Max, V_{OUT} = 0.5 V
I_{OS}	Output Current Short Circuit to Ground			−100	mA	V_{CC} = Max, *Note 3*
I_{CC}	Power Supply Current			65	mA	93L425-35, 93L425-45, 93L425-60 (commercial)
				75	mA	93L425-40, 93L425-50, 93L425-70 (military)
				125	mA	93425-25, 93425-30 (commercial)
				135	mA	93425-30, 93425-40 (military)
				155	mA	93425A, 93425-45 (commercial)
				170	mA	93425-60 (military) V_{CC} = Max, *Note 6*

Notes

1. Typical values are at V_{CC} = 5.0 V, T_C = +25°C and maximum loading.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
3. Short circuit to ground not to exceed one second.
4. t_W measured at t_{WSA} = Min. t_{WSA} measured at t_W = Min.
5. Static condition only.
6. All inputs GND
   Output open
7. I_{IL} = −300 μA for 93L425

Commercial

AC Performance Characteristics: $V_{CC} = 5.0 \pm 5\%$, GND = 0 V, $T_C = 0°$ C to $+75°$ C

Symbol	Characteristic	93425-20 93425-25		93425-30 93425A		93425-45		Unit	Condition
		Min	Max	Min	Max	Min	Max		
	Read Timing								
t_{ACS}	Chip Select Access Time		15		20		35	ns	*Figures 3a, 3b*
t_{ZRCS}	Chip Select to HIGH Z		20		20		35	ns	
t_{AA}	Address Access Time[2]		20/25		30		45	ns	
	Write Timing								
t_W	Write Pulse Width to Guarantee Writing[4]	15		20		35		ns	*Figure 4*
t_{WSD}	Data Setup Time Prior to Write	5		5		5		ns	
t_{WHD}	Data Hold Time after Write	5		5		5		ns	
t_{WSA}	Address Setup Time Prior to Write[4]	5		5		5		ns	
t_{WHA}	Address Hold Time after Write	5		5		5		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		5		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		5		ns	
t_{ZWS}	Write Enable to HIGH Z		15		20		35	ns	
t_{WR}	Write Recovery Time		15		20		40	ns	
t_{WR}	Write Recovery Time (93425A)				25			ns	

Military

AC Performance Characteristics: $V_{CC} = 5.0\ V \pm 10\%$, GND = 0 V, $T_C = -55°$ C to $+125°$ C

Symbol	Characteristic	93425-30		93425-40		93425-60		Unit	Condition
		Min	Max	Min	Max	Min	Max		
	Read Timing								
t_{ACS}	Chip Select Access Time		20		25		45	ns	*Figures 3a, 3b*
t_{ZRCS}	Chip Select to HIGH Z		20		25		50	ns	
t_{AA}	Address Access Time[2]		30		40		60	ns	
	Write Timing								
t_W	Write Pulse Width to Guarantee Writing[4]	20		25		40		ns	*Figure 4*
t_{WSD}	Data Setup Time Prior to Write	5		5		5		ns	
t_{WHD}	Data Hold Time after Write	5		5		5		ns	
t_{WSA}	Address Setup Time Prior to Write[4]	5		10		15		ns	
t_{WHA}	Address Hold Time after Write	5		5		5		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		5		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		5		ns	
t_{ZWS}	Write Enable to HIGH Z		20		25		45	ns	
t_{WR}	Write Recovery Time		20		25		50	ns	

Notes on preceding page

Commercial

AC Performance Characteristics: $V_{CC} = 5.0 \pm 5\%$, GND = 0 V, $T_C = 0°$ C to $+75°$ C

Symbol	Characteristic	93L425-35		93L425-45		93L425-60		Unit	Condition
		Min	Max	Min	Max	Min	Max		
	Read Timing								
t_{ACS}	Chip Select Access Time		25		30		40	ns	*Figures 3a, 3b*
t_{ZRCS}	Chip Select to HIGH Z		25		30		40	ns	
t_{AA}	Address Access Time[2]		35		45		60	ns	
	Write Timing								
t_W	Write Pulse Width to Guarantee Writing[4]	30		35		45		ns	
t_{WSD}	Data Setup Time Prior to Write	5		5		5		ns	
t_{WHD}	Data Hold Time after Write	5		5		5		ns	
t_{WSA}	Address Setup Time Prior to Write[4]	5		5		10		ns	*Figure 4a, 4b*
t_{WHA}	Address Hold Time after Write	5		5		5		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		5		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		5		ns	
t_{ZWS}	Write Enable to HIGH Z		20		25		45	ns	
t_{WR}	Write Recovery Time		30		35		45	ns	

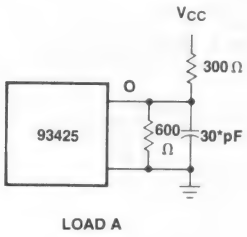
Military

AC Performance Characteristics: $V_{CC} = 5.0\ V \pm 10\%$, GND = 0 V, $T_C = -55°$ C to $+125°$ C

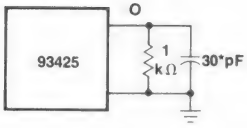
Symbol	Characteristic	93L425-40		93L425-50		93L425-70		Unit	Condition
		Min	Max	Min	Max	Min	Max		
	Read Timing								
t_{ACS}	Chip Select Access Time		30		35		45	ns	*Figures 3a, 3b*
t_{ZRCS}	Chip Select to HIGH Z		25		30		50	ns	
t_{AA}	Address Access Time[2]		40		50		70	ns	
	Write Timing								
t_W	Write Pulse Width to Guarantee Writing[4]	35		40		50		ns	
t_{WSD}	Data Setup Time Prior to Write	5		5		10		ns	
t_{WHD}	Data Hold Time after Write	5		5		10		ns	
t_{WSA}	Address Setup Time Prior to Write[4]	10		10		10		ns	*Figure 4a, 4b*
t_{WHA}	Address Hold Time after Write	5		5		10		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		10		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		5		ns	
t_{ZWS}	Write Enable to HIGH Z		25		30		45	ns	
t_{WR}	Write Recovery Time		30		40		55	ns	

Notes on page 4-27

Fig. 1 AC Test Output Load



LOAD A



LOAD B

*Includes jig and probe capacitance

Note: Load A is used for all production testing.

Fig. 2 AC Test Input Levels

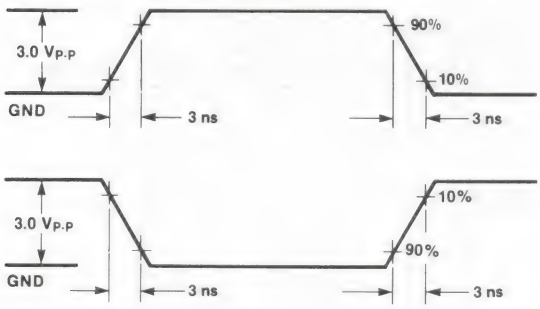
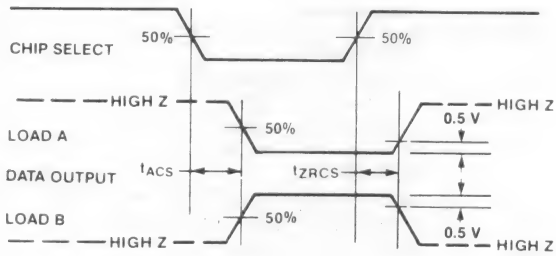


Fig. 3 Read Mode Timing

3a Read Mode Propagation Delay from Chip Select



3b Read Mode Propagation Delay from Address

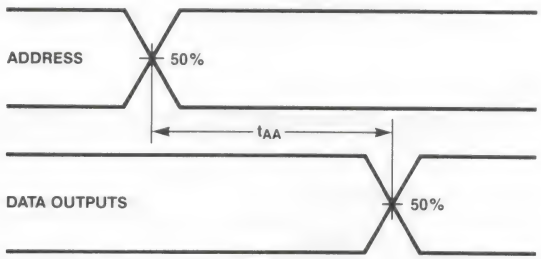
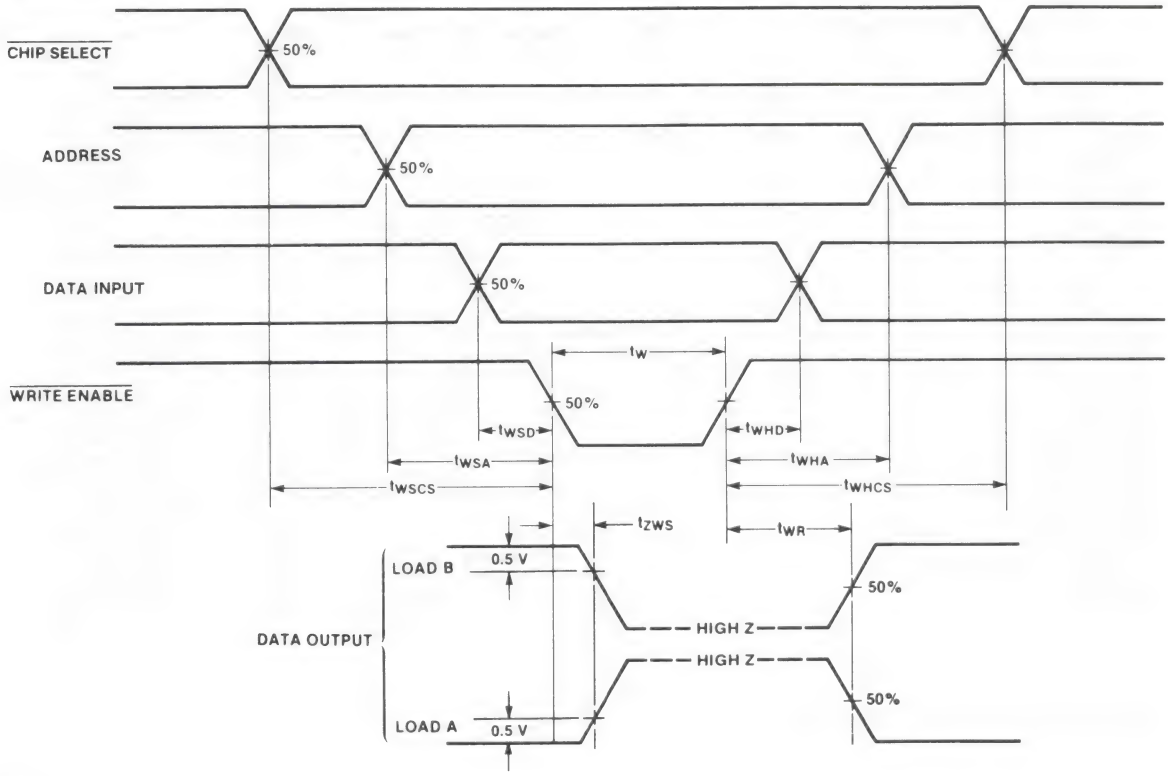


Fig. 4 Write Mode Timing



Notes

1. Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.
2. Input voltage levels for worst case AC test are 3.0/0.0 V.

Ordering Information

Part Number	Access Time (ns)	Power (mA)	Temperature Range	Package	Order Code
93425-20	20	125	0° C to +75° C	XX	93425XX20
93425-25	25	125	0° C to +75° C	XX	93425XX25
93425A	30	155	0° C to +75° C	XX	93425AXX
93425-30	30	125	0° C to +75° C	XX	93425XX30
93425-30	30	135	−55° C to +125° C	YY	93425YY30
93L425-35	35	65	0° C to +75° C	XX	93L425XX35
93425-40	40	135	−55° C to +125° C	YY	93425YY40
93L425-40	40	75	−55° C to +125° C	YY	93L425YY40
93425-45	45	155	0° C to +75° C	XX	93425XX
93L425-45	45	65	0° C to +75° C	XX	93L425XX45
93L425-50	50	75	−55° C to +125° C	YY	93L425YY50
93L425-60	60	65	0° C to +75° C	XX	93L425XX
93425-60	60	170	−55° C to +125° C	YY	93425YY
93L425-70	70	75	−55° C to +125° C	YY	93L425YY

Packages and Optional Processing (See Section 9)

XX — Commercial

Without Optional Processing	With Optional Processing
DC	DCQR — Ceramic Dip
FC	FCQR — Cerpak
PC	PCQR — Plastic Dip

YY — Military

Without Optional Processing	With Optional Processing
DM	DMQB — Ceramic Dip
FM	FMQB — Cerpak

Optional Processing

QB = Mil Std 883
Method 5004 and 5005, Level B
QR = Commercial Device with
160 Hour Burn in or Equivalent

Note:
Because every combination of packaging, speed, temperature, and optional processing is not in stock, availability of some combinations is not on an immediate basis.

FAIRCHILD
A Schlumberger Company

93479
256 x 9-Bit Static Random Access Memory

Memory and High Speed Logic

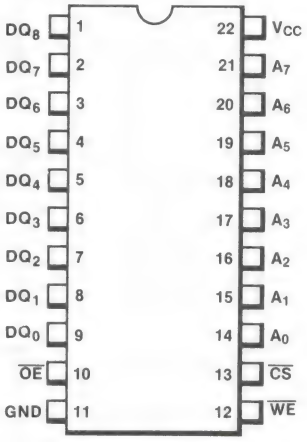
Description

The 93479 is a 2304-bit read/write Random Access Memory (RAM), organized as 256 words by nine bits per word. It is ideally suited for scratchpad, small buffer and other applications where the number of required words is small and where the number of required bits per word is relatively large. The ninth bit can be used to provide parity for 8-bit word systems.

- **Commercial Address Time**
  - **93479 — 45 ns Max**
  - **93479A — 35 ns Max**
- **Military Address Access Time**
  - **93479 — 60 ns Max**
  - **93479A — 45 ns Max**
- **Common Data Input/Output**
- **Features Three State Output**
- **Power Dissipation — 0.29 mW/Bit Typ**

Connection Diagram

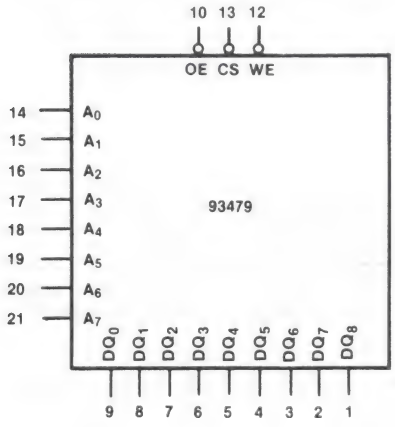
22-Pin DIP (Top View)



Pin Names

A_0-A_7	Address Inputs
DQ_0-DQ_8	Data Input/Outputs
$\overline{OE}$	Output Enable Input (Active LOW)
$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{CS}$	Chip Select Input (Active LOW)

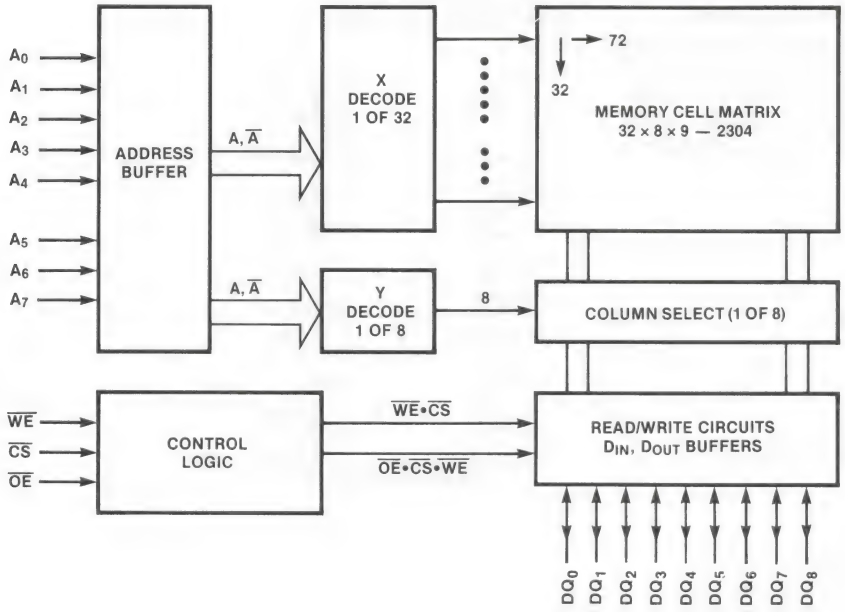
Logic Symbol



VCC = Pin 22
GND = Pin 11

4

Logic Diagram



Functional Description

The 93479 is a fully decoded 2304-bit random access memory organized 256 words by nine bits. Word selection is achieved by means of an 8-bit address, A_0 to A_7.

The Chip Select input provides for memory array expansion. For larger memories, the fast chip select access time permits decoding without an increase in overall memory access time.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW, the chip selected, and the output disabled, the data at DQ_0-DQ_8 is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH, the chip selected and the output enabled. Non-inverted data is then presented at the outputs DQ_0-DQ_8.

The 93479 has three-state outputs which provide an active pull-up or pull-down when enabled and a high impedance (HIGH Z) state when disabled. The active pull-ups provide drive capability for high capacative loads while the high impedance state allows optimization of word expansion in bus organized systems.

Truth Table

Inputs			Data In/Out	
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	DQ_0-DQ_8	Mode
X	H	X	HIGH Z	Output Disabled
H	X	X	HIGH Z	R/W Disabled
L	L	H	Data Out	Read
L	H	L	Data In	Write

H = HIGH Voltage Level (2.4 V)
L = LOW Voltage Level (.5 V)
X = Don't Care (HIGH or LOW)
HIGH Z = High Impedance State

DC Performance Characteristics: Over operating temperature ranges (Note 1)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition	
V_{OL}	Output LOW Voltage		0.3	0.5	V	V_{CC} = Min, I_{OL} = 8.0 mA	
V_{OH}	Output HIGH Voltage	2.4			V	V_{CC} = Min, I_{OH} = −5.2 mA	
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for All Inputs [5]	
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for All Inputs [5]	
I_{IL}	Input LOW Current		−250	−400	μA	V_{CC} = Max, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current		1.0	40	μA	V_{CC} = Max, V_{IN} = 4.5 V	
I_{IHB}	Input Breakdown Current			1.0	mA	V_{CC} = Max, V_{IN} = V_{CC}	
I_{OZH} I_{OZL}	Output Current (HIGH Z)		 −50	50 −400	μA μA	V_{CC} = Max, V_{OUT} = 2.4 V V_{CC} = Max, V_{OUT} = 0.5 V	
V_{IC}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = Max, I_{IN} = −10 mA	
I_{OS}	Output Current Short Circuit to Ground			−70	mA	V_{CC} = Max, Note 3	
I_{CC}	Power Supply Current			185 200	mA	Commercial Military	V_{CC} = Max All Inputs GND

Notes

1. Typical values are at V_{CC} = 5.0 V, T_C = +25° C and maximum loading.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
3. Short circuit to ground not to exceed one second.
4. t_W measured at t_{WSA} = Min. t_{WSA} measured at t_W = Min.
5. Static condition only.

4

Commercial

AC Performance Characteristics: $V_{CC} = 5.0\ V \pm 5\%$, GND = 0 V, $T_C = 0°C$ to $+75°C$

Symbol	Characteristic	A Min	A Max	Std Min	Std Max	Unit	Condition
	Read Timing						
t_{ACS}	Chip Select Access Time		25		25	ns	
t_{ZRCS}	Chip Select to HIGH Z		25		25	ns	
t_{AOS}	Output Enable Access Time		25		25	ns	*Figures 3a, 3b, 3c*
t_{ZROS}	Output Enable to HIGH Z		25		25	ns	
t_{AA}	Address Access Time[2]		35		45	ns	
	Write Timing						
t_W	Write Pulse Width to Guarantee Writing[4]	25		25		ns	
t_{SO}	Output Enable Setup Time	5		5		ns	
t_{HO}	Data Enable Hold Time	5		5		ns	
t_{WSD}	Data Setup Time Prior to Write	25		25		ns	*Figure 4*
t_{WHD}	Data Hold Time after Write	5		5		ns	
t_{WSA}	Address Setup Time Prior to Write[4]	5		5		ns	
t_{WHA}	Address Hold Time after Write	5		5		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		ns	

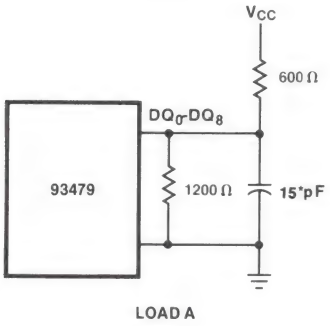
Military

AC Performance Characteristics: $V_{CC} = 5.0\ V \pm 10\%$, GND = 0 V, $T_C = -55°C$ to $+125°C$

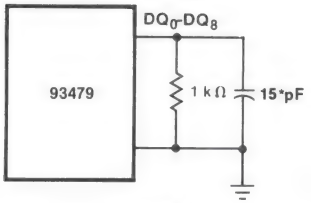
Symbol	Characteristic	A Min	A Max	Std Min	Std Max	Unit	Condition
	Read Timing						
t_{ACS}	Chip Select Access Time		30		40	ns	
t_{ZRCS}	Chip Select to HIGH Z		30		40	ns	
t_{AOS}	Output Enable Access Time		30		40	ns	*Figures 3a, 3b, 3c*
t_{ZROS}	Output Enable to HIGH Z		30		40	ns	
t_{AA}	Address Access Time[2]		45		60	ns	
	Write Timing						
t_W	Write Pulse Width to Guarantee Writing[4]	40		40		ns	
t_{SO}	Output Enable Setup Time	5		5		ns	
t_{HO}	Data Enable Hold Time	5		5		ns	
t_{WSD}	Data Setup Time Prior to Write	50		50		ns	*Figure 4*
t_{WHD}	Data Hold Time after Write	10		10		ns	
t_{WSA}	Address Setup Time Prior to Write[4]	10		10		ns	
t_{WHA}	Address Hold Time after Write	10		10		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	10		10		ns	
t_{WHCS}	Chip Select Hold Time after Write	10		10		ns	

Notes on preceding page

Fig. 1 AC Test Load Output Load



LOAD A



LOAD B

*Includes jig and probe capacitance

Note: Load A is used for all production testing.

Fig. 2 AC Test Input Levels

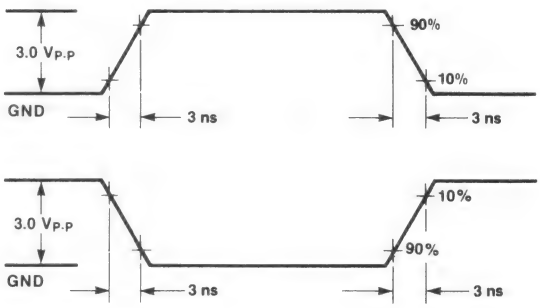
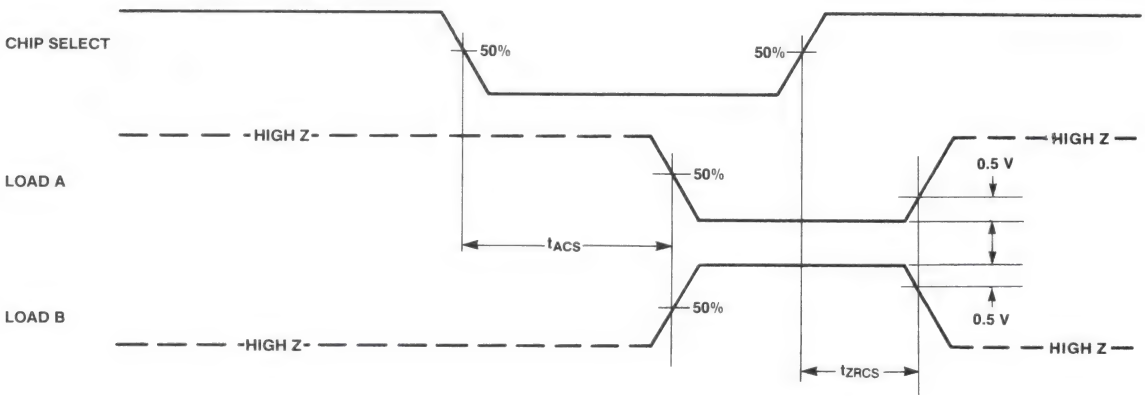
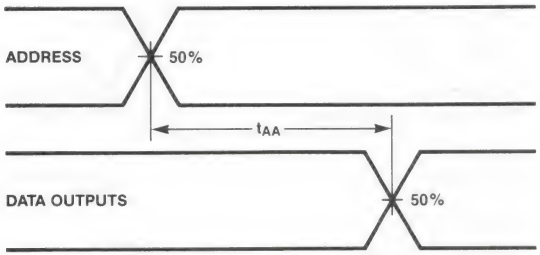


Fig. 3 Read Mode Timing

3a Read Mode Propagation Delay from Chip Select to Output



3b Read Mode Propagation Delay from Address to Output



3c Read Mode Propagation Delay from Output Enable

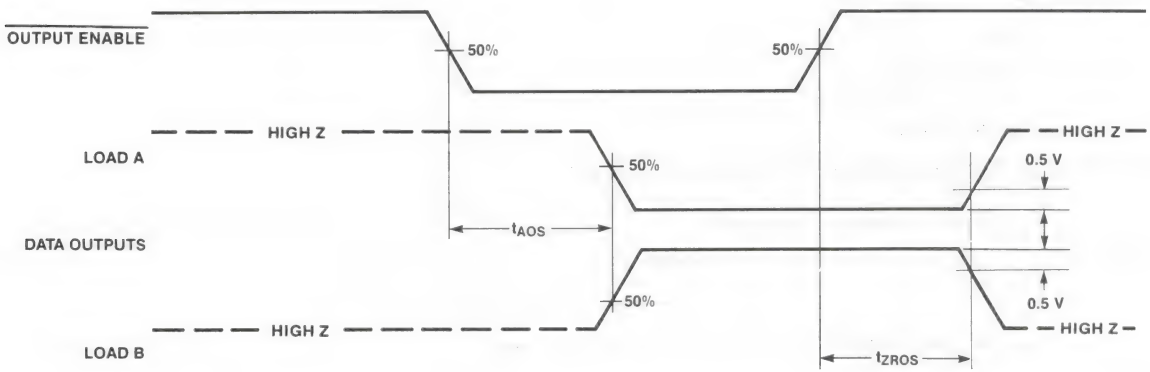
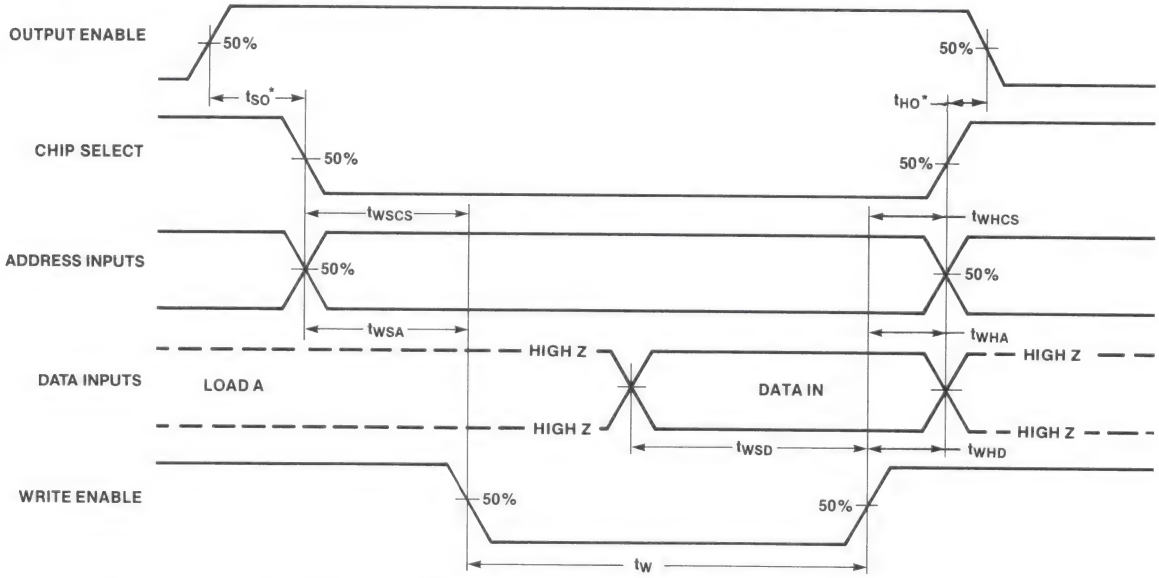


Fig. 4 Write Mode Timing

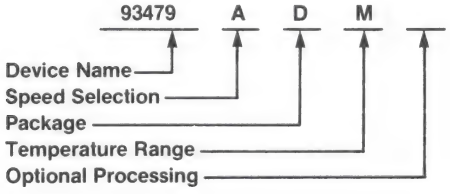


* These timing parameters are only necessary to guarantee High Z state during the entire write cycle

Notes

1. Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.
2. Input voltage levels for worst case AC test are 3.0/0.0 V.

Ordering Information



Speed Selection
Blank = Standard Speed
A = 'A' Grade

Packages and Outlines (See Section 9)
D = Ceramic DIP

Temperature Range
C = 0°C to +75°C
M = −55°C to +125°C

Optional Processing
QB = Mil Std 883
Method 5004 and 5005, Level B
QR = Commercial Device with
160 Hour Burn In or Equivalent

Notes

FAIRCHILD
A Schlumberger Company

F1600
65,536 x 1-Bit Static RAM

Description

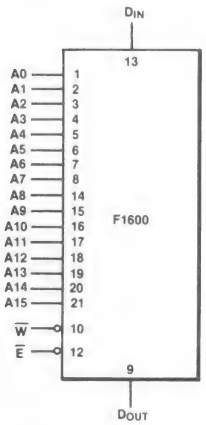
The F1600 is a 65,536-bit fully static asynchronous random access memory, organized as 65,536 words by 1-bit, using high-performance CMOS technology. The F1600 is based on an advanced isoplanar oxide isolation process: fully-implanted CMOS technology with sub-2 micron design rules and high-performance tantalum silicide gate electrodes. The high-density NMOS memory array and the CMOS peripheral circuits provide fast access time plus low active and standby power.

- **Single +5V Operation (±10%)**
- **Fully Static: No Clock or Timing Strobe Required**
- **Fast Access Time: 45 ns/55 ns/70 ns (Maximum)**
- **Low Power Dissipation:**
  - **70 mA Maximum (Active)**
  - **20 mA Maximum (Standby — TTL Input Levels)**
  - **5 mA Maximum (Standby — CMOS Input Levels)**
- **Directly TTL Compatible — All Inputs and Outputs**
- **Separate Data Input and Three-State Output**
- **Available in a 22-Pin DIP or LCC**
- **Polyimide Die Coat for Alpha Immunity**

Pin Names

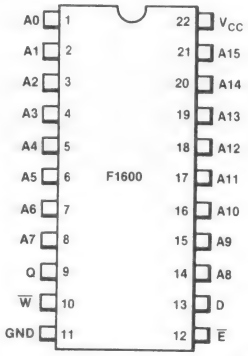
A_0-A_{15}	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output
V_{CC}	Power (5.0 V)
GND	Ground (0 V)

Logic Symbol

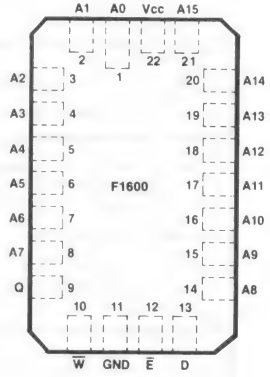


Connection Diagrams

22-Pin DIP (Top View)



22-Pin LCC (Top View)



5

Absolute Maximum Ratings

Voltage on Any Input or Output Pin With Respect to GND	– 2.0 V to 7.0 V
Storage Temperature	-55° C to +150° C
Operating Temperature	0° C to +70° C
Power Dissipation	1.0 W

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions: $T_C = 0°\,C$ to $+70°\,C$

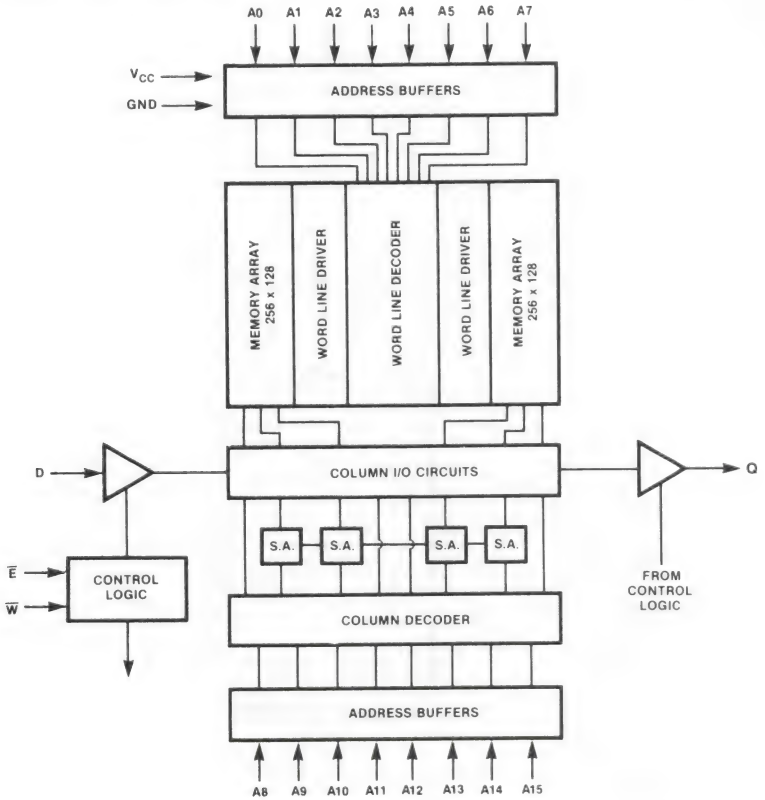
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		6.0	V
V_{IL}	Input LOW Voltage	-0.5*		0.8	V

All voltages are referenced to GND pin = 0 V.

*The device will withstand undershoots to -3.0 V of 20 ns duration. This is guaranteed by bench simulation in a DC mode, not 100% tested.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Functional Block Diagram



DC Operating Characteristics: $T_C = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 10\%$

Symbol	Characteristic	F1600-45			F1600-55			F1600-70			Unit	Condition
		Min	Typ.	Max	Min	Typ.	Max	Min	Typ.	Max		
I_{IN}	Input Leakage Current (All inputs)			±2			±2			±2	μA	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}
I_{OUT}	Output Leakage Current (on Q)			±2			±2			±2	μA	$\overline{E}$ = V_{IH} V_{OUT} = 0 V to V_{CC}
I_{CC1}	Operating Power Supply Current		40	70		40	70		40	70	mA	$\overline{E}$ = V_{IL}, Output Open
I_{CC2}	Dynamic Operating Supply Current		40	70		40	70		40	70	mA	Min. Read Cycle Time Duty Cycle = 100% Output Open
I_{SB1}	Standby Supply Current		5	20		5	20		5	20	mA	$\overline{E} \geq V_{IH}$, see *note 1*
I_{SB2}	Full Standby Supply Current		0.02	5.0		0.02	5.0		0.02	5.0	mA	see *note 2*
I_{OS}	Output Current Short Circuit to Ground			−125			−125			−125	mA	V_{CC} = 5.5 V Duration not to Exceed 1 Second
V_{OL}	Output LOW Voltage			0.4			0.4			0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output HIGH Voltage	2.4			2.4			2.4			V	I_{OH} = -4.0 mA

AC Test Conditions[3]

Input Pulse Levels ..... GND to 3.0 V
Input Rise and Fall Times ..... 5 ns
Input and Output Timing Reference Levels ..... 1.5 V
Output Load ..... *See Figures 1 and 2*

Capacitance[4] $T_C = +25°C$, f = 1.0 MHz

Symbol	Parameter	Max.	Units	Conditions
C_{IN}	Input Capacitance	5	pF	V_{IN} = 0 V
C_{OUT}	Output Capacitance	6	pF	V_{OUT} = 0 V

Effective capacitance calculated from the equation

$C = \frac{\Delta Q}{\Delta V}$ where $\Delta V = 3$ V.

Truth Table

Mode	$\overline{E}$	$\overline{W}$	D	Q	Power Level
Standby	H	X	X	HIGH Z	Standby
Read	L	H	X	D	Active
Write	L	L	D	HIGH Z	Active

HIGH Z = High impedance
D = Valid data bit
X = Don't care

Figure 1 Output Load

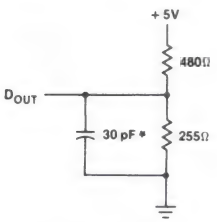
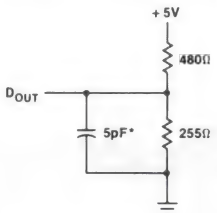


Figure 2 Output Load (for t_{EHQZ}, t_{ELQX}, t_{WLQZ}, t_{WHQX})



*Including scope and jig.

Notes on page 5-9

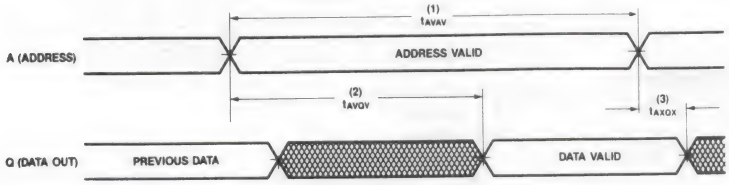
AC Operating Conditions and Characteristics: Read Cycle $T_C = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 10\%$

No.	Symbol		Parameter	F1600-45		F1600-55		F1600-70		Unit	Notes
	Standard	Alternate		Min	Max	Min	Max	Min	Max		
1	t_{AVAV}	t_{RC}	Address Valid to Address Valid (Read Cycle Time)	45		55		70		ns	5,6,9
2	t_{AVQV}	t_{AA}	Address Valid to Output Valid (Address Access Time)		45		55		70	ns	5
3	t_{AXQX}	t_{OH}	Address Invalid to Output Invalid (Output Hold Time)	5		5		5		ns	
4	t_{ELEH}	t_{RC}	Chip Enable LOW to Chip Enable HIGH (Read Cycle Time)	45		55		70		ns	6,9
5	t_{ELQV}	t_{ACS}	Chip Enable LOW to Output Valid (Chip Enable Access Time)		45		55		70	ns	6
6	t_{ELQX}	t_{LZ}	Chip Enable LOW to Output Invaild (Chip Enable to Output Active)	0		0		0		ns	4
7	t_{EHQZ}	t_{HZ}	Chip Enable HIGH to Output High Z (Chip Disable to Output Disable)	0	20	0	25	0	30	ns	4, 10
8	t_{ELICCH}	t_{PU}	Chip Enable LOW to Power Up	0		0		0		ns	4
9	t_{EHICCL}	t_{PD}	Chip Enable HIGH to Power Down		40		40		40	ns	4

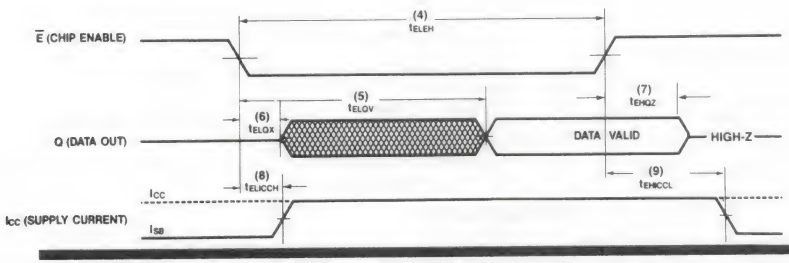
Notes on page 5-9

Timing Waveforms

Read Cycle 1 (Where $\overline{E}$ is active prior to address change. $\overline{W}$ = HIGH)



Read Cycle 2 (Where address is valid prior to $\overline{E}$ becoming active. $\overline{W}$ = HIGH)

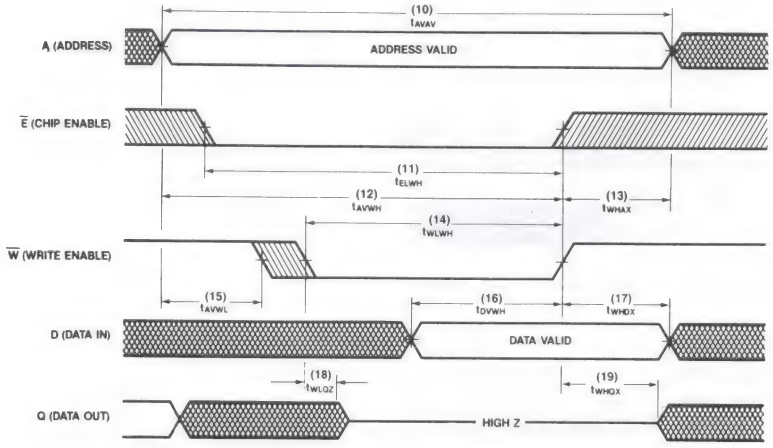


AC Operating Conditions and Characteristics: Write Cycle 1 $T_C = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 10\%$

No.	Symbol		Parameter	F1600-45		F1600-55		F1600-70		Unit	Notes
	Standard	Alternate		Min	Max	Min	Max	Min	Max		
10	t_{AVAV}	t_{WC}	Address Valid to Address Valid (Write Cycle Time)	45		55		70		ns	7,8,9
11	t_{ELWH}	t_{CW}	Chip Enable to Write HIGH (Chip Enable to End of Write)	40		45		55		ns	11
12	t_{AVWH}	t_{AW}	Address Valid to Write HIGH (Address Setup to End of Write)	40		45		55		ns	11
13	t_{WHAX}	t_{WR}	Write HIGH to Address Don't Care (Address Hold After End of Write)	0		0		0		ns	11
14	t_{WLWH}	t_{WP}	Write LOW to Write HIGH (Write Pulse Width)	20		25		40		ns	11
15	t_{AVWL}	t_{AS}	Address Valid to Write LOW (Address Setup to Beginning of Write)	5		5		5		ns	11
16	t_{DVWH}	t_{DW}	Data Valid to Write HIGH (Data Setup to End of Write)	15		20		30		ns	11
17	t_{WHDX}	t_{DH}	Write HIGH to Data Don't Care (Data Hold After End of Write)	0		0		0		ns	11
18	t_{WLQZ}	t_{WZ}	Write LOW to Output High Z (Write Enable to Output Disable)	0	20	0	25	0	30	ns	4, 10
19	t_{WHQX}	t_{OW}	Write HIGH to Output Don't Care (Output Active After End of Write)	0		0		0		ns	4

Notes on page 5-9

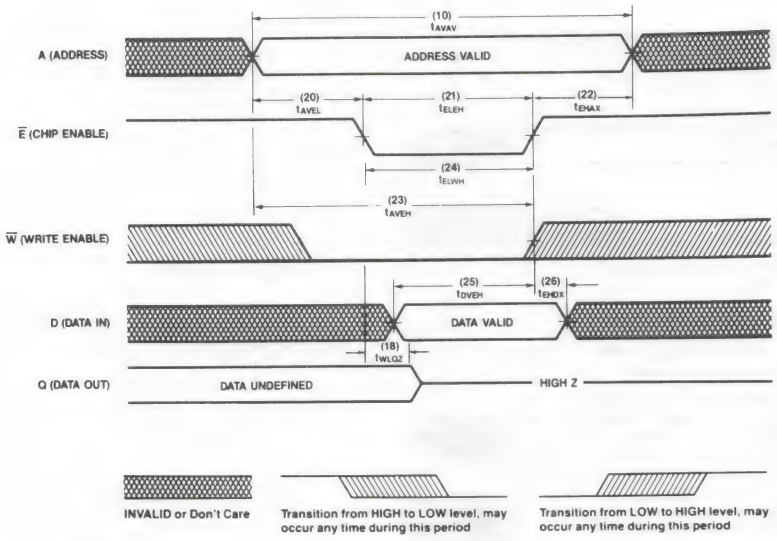
Write Cycle 1 ($\overline{W}$ controlled, where $\overline{E}$ is active prior to $\overline{W}$ becoming active.)



AC Operating Conditions and Characteristics: Write Cycle 2 $T_C = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 10\%$

No.	Symbol		Parameter	F1600-45		F1600-55		F1600-70		Unit	Notes
	Standard	Alternate		Min	Max	Min	Max	Min	Max		
20	t_{AVEL}	t_{AS}	Address Valid to Chip Enable LOW (Address Set Up)	0		0		0		ns	
21	t_{ELEH}	t_{CW}	Chip Enable LOW to Chip Enable HIGH (Write Cycle Time)	45		55		70		ns	11
22	t_{EHAX}	t_{WR}	Chip Enable HIGH to Address Don't Care (Address Hold After End of Write)	0		0		0		ns	
23	t_{AVEH}	t_{AW}	Address Valid to Chip Enable HIGH (Address Setup to End of Write)	40		45		55		ns	
24	t_{ELWH}	t_{WP}	Chip Enable LOW to Write HIGH (Write Pulse Width)	30		35		40		ns	11
25	t_{DVEH}	t_{DW}	Data Valid to Chip Enable HIGH (Data Setup to End of Write)	15		20		30		ns	
26	t_{EHDX}	t_{DH}	Chip Enable HIGH to Data Don't Care (Data Hold)	0		0		0		ns	

Write Cycle 2 ($\overline{E}$ controlled, where $\overline{W}$ is active prior to $\overline{E}$ becoming active. *See Note 9.*)



Notes on page 5-9

Notes

1. This parameter is measured with $\overline{E}$ HIGH (chip deselected) and inputs at valid TTL levels.
2. This parameter is measured with input levels either $\geq V_{CC} - 0.2$ V or ≤ 0.2 V, including $\overline{E}$ which must be $\geq V_{CC} - 0.2$ V. This condition results in significant reduction in current in the input buffer circuitry and consequently a lower overall current level.
3. Operation to specifications guaranteed 2.0 ms after V_{CC} applied.
4. This parameter is sampled and not 100% tested.
5. Read Cycle 1 assumes that Chip Enable (E) occurs before the addresses are valid. Timing considerations are referenced to the edges of Address Valid.
6. Read Cycle 2 assumes that Address Valid occurs prior to Chip Enable ($\overline{E}$). Timing considerations are referenced to the edges of Chip Enable.
7. Since a write cycle can only occur during intervals where both $\overline{E}$ and $\overline{W}$ are LOW, Write Cycle 1 assumes that $\overline{W}$ is the latter of the two signals to go LOW (active) and is also the first of the two signals to go HIGH (inactive). Consequently, timing considerations are referenced to the edges of $\overline{W}$ rather than $\overline{E}$.
8. Write Cycle 2 assumes that, of the two control signals, $\overline{E}$ and $\overline{W}$. $\overline{E}$ is the latter of the two to go LOW (active) and is also the first of the two to go HIGH (inactive). Consequently, timing considerations are referenced to the edges of $\overline{E}$ rather than $\overline{W}$.
9. All READ and WRITE cycle timings are referenced from the last bit to become valid address to the first transitioning address.
10. Transition to high impedance state is measured ±500 mV from steady state voltage with specified loading in *Figure 2*. This parameter is sampled, not 100% tested.
11. Since Write Enable ($\overline{W}$) is gated internally with Chip Enable ($\overline{E}$), the value of $\overline{W}$ during periods where $\overline{E}$ is HIGH is irrelevant (i.e., don't care). Thus, whenever $\overline{W}$ transitions to the LOW state prior to $\overline{E}$, all timing references will be to the falling edge of $\overline{E}$ rather than $\overline{W}$. Similarly, whenever $\overline{E}$ transitions to the HIGH state prior to $\overline{W}$, all timing references will be to the rising edge of $\overline{E}$ rather than $\overline{W}$.
12. Input pulse levels 0 to 3.0 Volts.
13. Input rise and fall times are assumed to be 5 ns. Timing measurement reference levels are 1.5 Volts.
14. Rise and fall times should not exceed 45 ns.

Ordering Information

Part Number	Access Time	Temperature Range	Package	Order Code
F1600-45	45 ns	0°C to + 70°C	Side-brazed	1600DC45
F1600-45	45 ns	0°C to + 70°C	Leadless Chip Carrier	1600LC45
F1600-45	45 ns	0°C to + 70°C	Plastic DIP	1600PC45
F1600-55	55 ns	0°C to + 70°C	Side-brazed	1600DC55
F1600-55	55 ns	0°C to + 70°C	Leadless Chip Carrier	1600LC55
F1600-55	55 ns	0°C to + 70°C	Plastic DIP	1600PC55
F1600-70	70 ns	0°C to + 70°C	Side-brazed	1600DC70
F1600-70	70 ns	0°C to + 70°C	Leadless Chip Carrier	1600LC70
F1600-70	70 ns	0°C to + 70°C	Plastic DIP	1600PC70

FAIRCHILD
A Schlumberger Company

F1600
65,536 x 1-Bit Static RAM
Military Temperature Range

Memory and High Speed Logic

Description

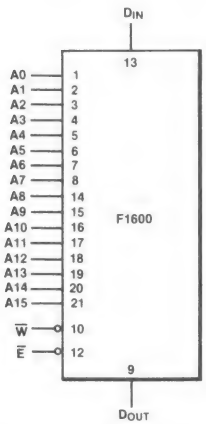
The F1600 is a 65,536-bit fully static asynchronous random access memory, organized as 65,536 words by 1-bit, using high-performance CMOS technology. The F1600 is based on an advanced isoplanar oxide isolation process: fully-implanted CMOS technology with sub-2 micron design rules and high-performance tantalum silicide gate electrodes. The high-density NMOS memory array and the CMOS peripheral circuits provide fast access time plus low active and standby power.

- **Single +5V Operation (±10%)**
- **Fully Static: No Clock or Timing Strobe Required**
- **Fast Access Time: 55 ns/70 ns (Maximum)**
- **Specifications Guaranteed Over Full Military Temperature Range (-55°C to+125°C)**
- **Low Power Dissipation :**
  - **70 mA Maximum (Active)**
  - **20 mA Maximum (Standby — TTL Input Levels)**
  - **9 mA Maximum (Standby — CMOS Input Levels)**
- **Directly TTL Compatible — All Inputs and Outputs**
- **Separate Data Input and Three-State Output**
- **Available in a 22-Pin DIP or LCC**
- **Polyimide Die Coat for Alpha Immunity**

Pin Names

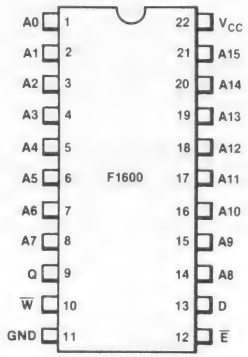
A_0-A_{15}	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output
V_{CC}	Power (5.0 V)
GND	Ground (0 V)

Logic Symbol

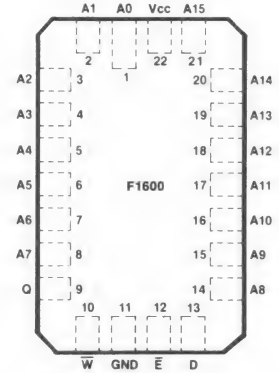


Connection Diagrams

22-Pin DIP (Top View)



22-Pin LCC (Top View)



Absolute Maximum Ratings

Voltage on Any Input or Output Pin With Respect to GND	-2.0 V to 7.0 V
Storage Temperature Range	-65° C to +150° C
Operating Temperature Range	−55°C to +125°C
Power Dissipation	1.0 W
Maximum Junction Temperature (T_J)	+150°C
Thermal Resistance, Junction to Case (θ_{JC}): Case (Side-Brazed DIP)	15°C/W

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condition for extended periods may affect device reliability.

Recommended Operating Conditions: T_C = -55°C to +125°C

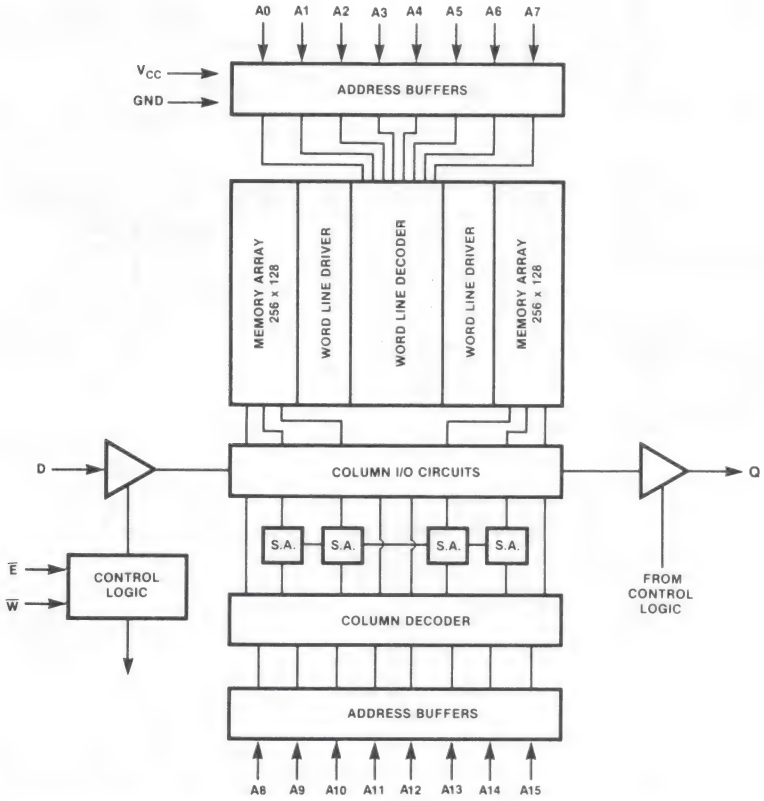
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		6.0	V
V_{IL}	Input LOW Voltage	-0.5*		0.8	V

All voltages are referenced to GND pin = 0 V.

*The device will withstand undershoots to -3.0 V of 20 ns duration. This is guaranteed by bench simulation in a DC mode, not 100% tested.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Functional Block Diagram



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DC Operating Characteristics: T_C = -55° C to +125° C, V_{CC} = 5.0V ±10%

Symbol	Characteristic	F1600-55 Min	F1600-55 Max	F1600-70 Min	F1600-70 Max	Unit	Condition
I_{IN}	Input Leakage Current (All inputs)		±5		±5	uA	V_{CC} = 5.5 V, V_{IN} = 0 V and 5.5 V
I_{OUT}	Output Leakage Current (on Q)		±10		±10	uA	$\overline{E} = V_{IH}$ V_{OUT} = 0 V and 5.5 V
I_{CC1}	Operating Power Supply Current		70		70	mA	$\overline{E} = V_{IL}$, Output Open
I_{CC2}	Dynamic Operating Supply Current		70		70	mA	Min. Read Cycle Time Duty Cycle = 100% Output Open
I_{SB1}	Standby Supply Current		20		20	mA	$\overline{E} \geq V_{IH}$, see *note 1*
I_{SB2}	Full Standby Supply Current		9.0		9.0	mA	see *note 2*
I_{OS}	Output Current Short Circuit to Ground		-135		-135	mA	V_{CC} = 5.5 V Duration not to Exceed 1 Second
V_{OL}	Output LOW Voltage		0.4		0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output HIGH Voltage	2.4		2.4		V	I_{OH} = −4.0 mA

AC Test Conditions[3]

Input Pulse Levels ..... GND to 3.0 V
Input Rise and Fall Times ..... 5 ns
Input and Output Timing Reference Levels ..... 1.5 V
Output Load ..... *See Figures 1 and 2*

Capacitance[4] T_C = +25°C, f = 1.0 MHz

Symbol	Parameter	Max.	Units	Conditions
C_{IN}	Input Capacitance	5	pF	V_{IN} = 0 V
C_{OUT}	Output Capacitance	6	pF	V_{OUT} = 0 V

Effective capacitance calculated from the equation

$C = \frac{\Delta Q}{\Delta V}$ where $\Delta V = 3$ V.

Truth Table[5]

Mode	$\overline{E}$	$\overline{W}$	D	Q	Power Level
Standby	H	X	X	HIGH Z	Standby
Read	L	H	X	D	Active
Write	L	L	D	HIGH Z	Active

HIGH Z – High impedance
D – Valid data bit
X – Don't care

Figure 1 Output Load

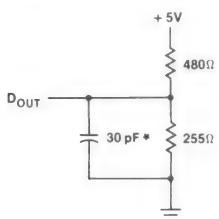
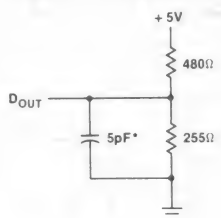


Figure 2 Output Load (for t_{EHQZ}, t_{ELQX}, t_{WLQZ}, t_{WHQX})



*Including scope and jig.

Notes on page 5-16

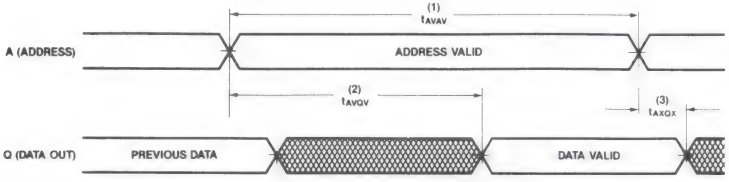
AC Operating Conditions and Characteristics: Read Cycle T_C = -55° C to +125° C, V_{CC} = 5.0V ±10%

No.	Symbol		Parameter	F1600-55		F1600-70		Unit	Notes
	Standard	Alternate		Min	Max	Min	Max		
1	t_{AVAV}	t_{RC}	Address Valid to Address Valid (Read Cycle Time)	55		70		ns	6,7,10
2	t_{AVQV}	t_{AA}	Address Valid to Output Valid (Address Access Time)		55		70	ns	6
3	t_{AXQX}	t_{OH}	Address Invalid to Output Invalid (Output Hold Time)	5		5		ns	
4	t_{ELEH}	t_{RC}	Chip Enable LOW to Chip Enable HIGH (Read Cycle Time)	55		70		ns	7,10
5	t_{ELQV}	t_{ACS}	Chip Enable LOW to Output Valid (Chip Enable Access Time)		55		70	ns	7
6	t_{ELQX}	t_{LZ}	Chip Enable LOW to Output Invalid (Chip Enable to Output Active)	0		0		ns	4
7	t_{EHQZ}	t_{HZ}	Chip Enable HIGH to Output High Z (Chip Disable to Output Disable)	0	35	0	40	ns	4, 11
8	t_{ELICCH}	t_{PU}	Chip Enable LOW to Power Up	0		0		ns	4
9	t_{EHICCL}	t_{PD}	Chip Enable HIGH to Power Down		45		45	ns	4

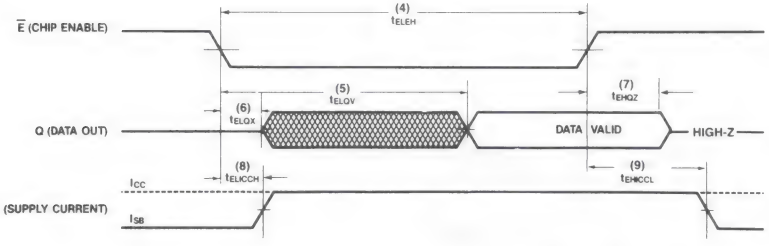
Notes on page 5-16

Timing Waveforms

Read Cycle 1 (Where $\overline{E}$ is active prior to address change. $\overline{W}$ = HIGH)



Read Cycle 2 (Where address is valid prior to $\overline{E}$ becoming active. $\overline{W}$ = HIGH)

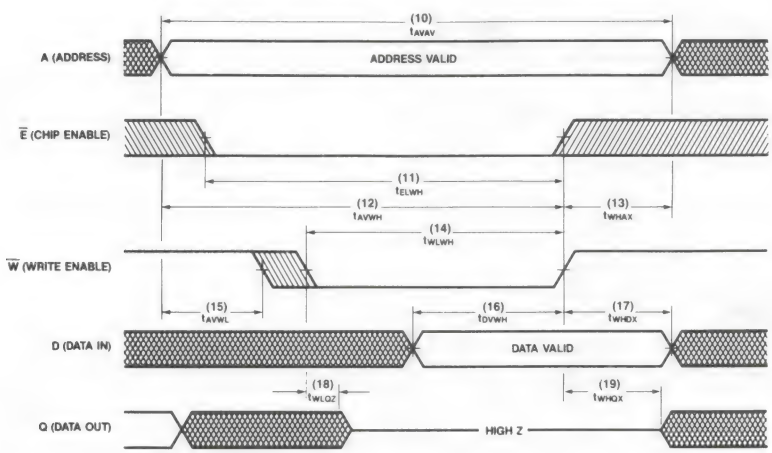


AC Operating Conditions and Characteristics: Write Cycle 1 T_C = -55° C to +125° C, V_{CC} = 5.0V ±10%

No.	Symbol		Parameter	F1600-55		F1600-70		Unit	Notes
	Standard	Alternate		Min	Max	Min	Max		
10	t_{AVAV}	t_{WC}	Address Valid to Address Valid (Write Cycle Time)	55		70		ns	8,9,10
11	t_{ELWH}	t_{CW}	Chip Enable to Write HIGH (Chip Enable to End of Write)	50		55		ns	12
12	t_{AVWH}	t_{AW}	Address Valid to Write HIGH (Address Setup to End of Write)	50		55		ns	12
13	t_{WHAX}	t_{WR}	Write HIGH to Address Don't Care (Address Hold After End of Write)	5		5		ns	12
14	t_{WLWH}	t_{WP}	Write LOW to Write HIGH (Write Pulse Width)	35		40		ns	12
15	t_{AVWL}	t_{AS}	Address Valid to Write LOW (Address Setup to Beginning of Write)	15		15		ns	12
16	t_{DVWH}	t_{DW}	Data Valid to Write HIGH (Data Setup to End of Write)	25		30		ns	12
17	t_{WHDX}	t_{DH}	Write HIGH to Data Don't Care (Data Hold After End of Write)	5		5		ns	12
18	t_{WLQZ}	t_{WZ}	Write LOW to Output High Z (Write Enable to Output Disable)	0	30	0	35	ns	4, 11
19	t_{WHQZ}	t_{OW}	Write HIGH to Output Don't Care (Output Active After End of Write)	0		0		ns	4

Notes on page 5-16

Write Cycle 1 ($\overline{W}$ controlled, where $\overline{E}$ is active prior to $\overline{W}$ becoming active.)



AC Operating Conditions and Characteristics: Write Cycle 2 T_C = -55° C to +125° C, V_{CC} = 5.0V ±10%

No.	Symbol		Parameter	F1600-55		F1600-70		Unit	Notes
	Standard	Alternate		Min	Max	Min	Max		
20	t_{AVEL}	t_{AS}	Address Valid to Chip Enable LOW (Address Set Up)	5		5		ns	
21	t_{ELEH}	t_{CW}	Chip Enable LOW to Chip Enable HIGH (Write Cycle Time)	55		70		ns	12
22	t_{EHAX}	t_{WR}	Chip Enable HIGH to Address Don't Care (Address Hold After End of Write)	5		5		ns	
23	t_{AVEH}	t_{AW}	Address Valid to Chip Enable HIGH (Address Setup to End of Write)	50		65		ns	
24	t_{ELWH}	t_{WP}	Chip Enable LOW to Write HIGH (Write Pulse Width)	35		40		ns	12
25	t_{DVEH}	t_{DW}	Data Valid to Chip Enable HIGH (Data Setup to End of Write)	25		30		ns	
26	t_{EHDX}	t_{DH}	Chip Enable HIGH to Data Don't Care (Data Hold)	5		5		ns	

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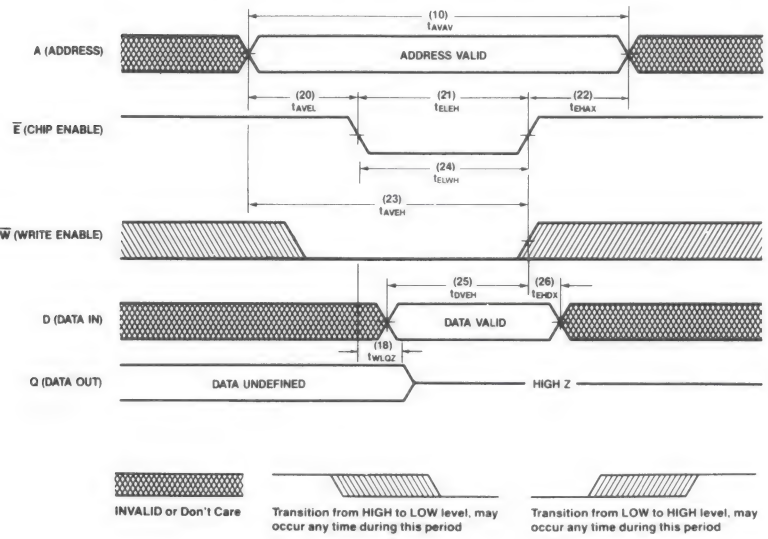
Write Cycle 2 ($\overline{E}$ controlled, where $\overline{W}$ is active prior to $\overline{E}$ becoming active. *See Note 9.)*



Notes on page 5-16

Notes

1. This parameter is measured with Chip Enable ($\overline{E}$) HIGH and inputs at valid TTL levels (0.5 V and 2.5 V).
2. This parameter is measured with input levels either $\geq V_{CC} - 0.2$ V or ≤ 0.2 V, including $\overline{E}$ which must be $\geq V_{CC} - 0.2$ V. This condition results in significant reduction in current in the input buffer circuitry and consequently a lower overall current level.
3. Operation to specifications guaranteed 2.0 ms after V_{CC} applied.
4. This parameter value is based on initial design qualification and is also verified on every design change. These are not tested in production.
5. Function test performed with the following input conditions: $V_{IL} = 0.4$ V and $V_{IH} = 2.4$.
6. Read Cycle 1 assumes that Chip Enable ($\overline{E}$) occurs before the addresses are valid. Timing considerations are referenced to the edges of Address Valid.
7. Read Cycle 2 assumes that Address Valid occurs prior to Chip Enable ($\overline{E}$). Timing considerations are referenced to the edges of Chip Enable.
8. Since a write cycle can only occur during intervals where both $\overline{E}$ and $\overline{W}$ are LOW, Write Cycle 1 assumes that $\overline{W}$ is the latter of the two signals to go LOW (active) and is also the first of the two signals to go HIGH (inactive). Consequently, timing considerations are referenced to the edges of $\overline{W}$ rather than $\overline{E}$.
9. Write Cycle 2 assumes that, of the two control signals, $\overline{E}$ and $\overline{W}$, $\overline{E}$ is the latter of the two to go LOW (active) and is also the first of the two to go HIGH (inactive). Consequently, timing considerations are referenced to the edges of $\overline{E}$ rather than $\overline{W}$.
10. All READ and WRITE cycle timings are referenced from the last bit to become valid address to the first transitioning address.
11. Transition to high impedance state is measured ±500 mV from steady state voltage with specified loading in *Figure 2*.
12. Since Write Enable ($\overline{W}$) is gated internally with Chip Enable ($\overline{E}$), the value of $\overline{W}$ during periods where $\overline{E}$ is HIGH is irrelevant (i.e., don't care). Thus, whenever $\overline{W}$ transitions to the LOW state prior to $\overline{E}$, all timing references will be to the falling edge of $\overline{E}$ rather than $\overline{W}$. Similarly, whenever $\overline{E}$ transitions to the HIGH state prior to $\overline{W}$, all timing references will be to the rising edge of E rather than $\overline{W}$.
13. Input pulse levels 0 to 3.0 Volts.
14. Input rise and fall times are assumed to be 5 ns. Timing measurement reference levels are 1.5 Volts.
15. Rise and fall times should not exceed 45 ns.

Ordering Information

Part Number	Access Time	Temperature Range	Package	Order Code
F1600-55	55 ns	−55°C to +125°C	Side-brazed	1600DMQB55
F1600-55	55 ns	−55°C to +125°C	Leadless Chip Carrier	1600LMQB55
F1600-70	70 ns	−55°C to +125°C	Side-brazed	1600DMQB70
F1600-70	70 ns	−55°C to +125°C	Leadless Chip Carrier	1600LMQB70

FAIRCHILD
A Schlumberger Company

F1601
65,546 x 1-Bit Static RAM
Data Retention Version

Description

The F 1601 is a 65,536-bit fully static asynchronous random access memory, organized as 65,536 words by 1-bit, using high-performance CMOS technology. The F1601 is based on an advanced isoplanar oxide isolation process; fully-implanted CMOS technology with sub-2 micron design rules and high-performance tantalum silicide gate electrodes. The high-density NMOS memory array and the CMOS peripheral circuits provide fast access time plus low active and standby power.

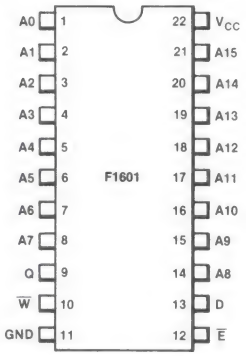
- **Single +5V Operation (±10%)**
- **Fast Access Time: 45 ns/55 ns/70 ns (Maximum)**
- **Power Dissipation (Normal Operation):**
  70 mA Maximum (Active)
  20 mA Maximum (Standby — TTL Input Levels)
  2 mA Maximum (Standby — CMOS Input Levels)
- **Data Retention Supply Voltage**
  2.0V to 5.5V
- **Low Power Dissipation (Data Retention)**
  $I_{CCDR} = 50\ \mu A$ Maximum ($2.0\ V \leq V_{DR} \leq 3.0\ V$)
- **Fully Static: No Clock or Timing Strobe Required**
- **Directly TTL Compatible — All Inputs and Outputs**
- **Separate Data Input and Three-State Output**
- **Available in a 22-Pin DIP or LCC**
- **Polyimide Die Coat for Alpha Immunity**

Pin Names

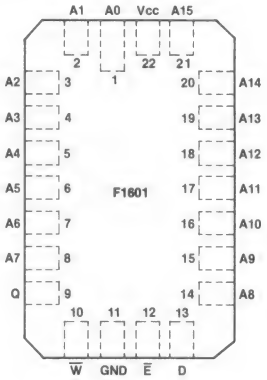
A_0-A_{15}	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output
V_{CC}	Power (5.0 V)
GND	Ground (0 V)

Connection Diagrams

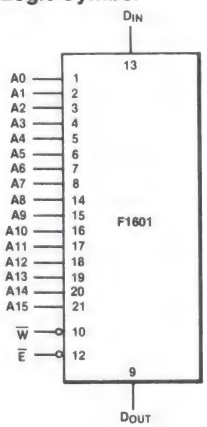
22-Pin DIP (Top View)



22-Pin LCC (Top View)



Logic Symbol



5

Absolute Maximum Ratings

Voltage on Any Input or Output Pin With Respect to GND	-2.0V to +7.0V
Storage Temperature	-55° C to +150° C
Operating Temperature	0° C to +70° C
Power Dissipation	1.0W

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions: T_C = 0° C to +70° C

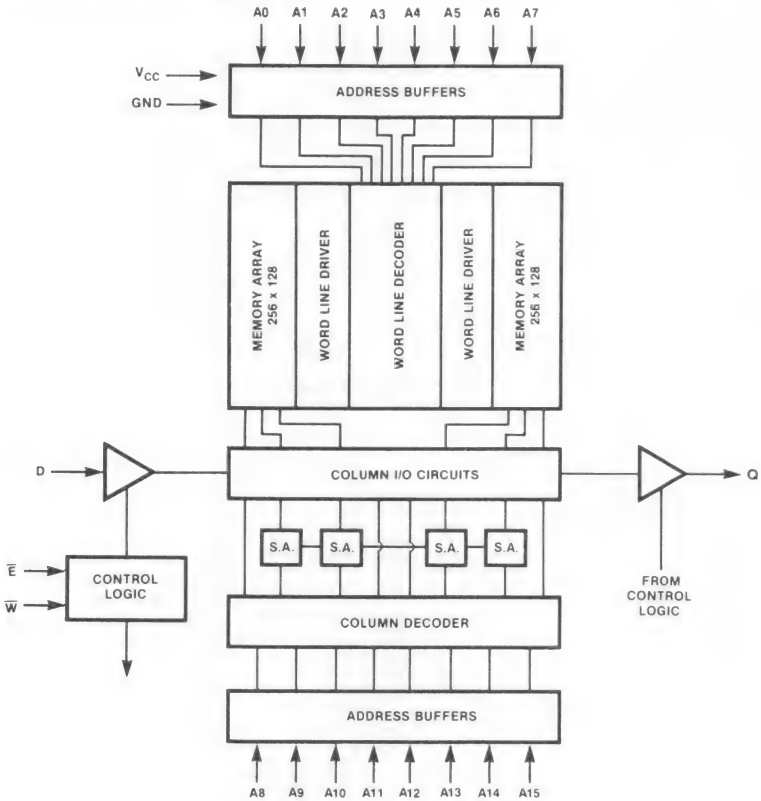
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		6.0	V
V_{IL}	Input LOW Voltage	-0.5*		0.8	V

All voltages are referenced to GND pin = 0 V.

*The device will withstand undershoots to -3.0 V of 20 ns duration. This is guaranteed by bench simulation in a DC mode, not 100% tested.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Functional Block Diagram



DC Operating Characteristics: $T_C = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 10\%$

Symbol	Characteristic	F1601-45			F1601-55			F1601-70			Unit	Condition
		Min	Typ.	Max	Min	Typ.	Max	Min	Typ.	Max		
I_{IN}	Input Leakage Current (All inputs)			± 2			± 2			± 2	μA	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}
I_{OUT}	Output Leakage Current (on Q)			± 2			± 2			± 2	μA	$\overline{E}$ = V_{IH} V_{OUT} = 0 V to V_{CC}
I_{CC1}	Operating Power Supply Current		40	70		40	70		40	70	mA	$\overline{E}$ = V_{IL}, Output Open
I_{CC2}	Dynamic Operating Supply Current		40	70		40	70		40	70	mA	Min. Read Cycle Time Duty Cycle = 100% Output Open
I_{SB1}	Standby Supply Current		5	20		5	20		5	20	mA	$\overline{E} \geq V_{IH}$, see *note 1*
I_{SB2}	Full Standby Supply Current		0.02	2.0		0.02	2.0		0.02	2.0	mA	see *note 2*
I_{OS}	Output Current Short Circuit to Ground			-125			-125			-125	mA	V_{CC} = 5.5 V Duration not to Exceed 1 Second
V_{OL}	Output LOW Voltage			0.4			0.4			0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output HIGH Voltage	2.4			2.4			2.4			V	I_{OH} = -4.0 mA

AC Test Conditions[3]

Input Pulse Levels ..... GND to 3.0 V
Input Rise and Fall Times ..... 5 ns
Input and Output Timing Reference Levels ..... 1.5 V
Output Load ..... *See Figures 1 and 2*

Capacitance[4]: $T_C = +25°C$, f = 1.0MHz

Symbol	Parameter	Max.	Units	Conditions
C_{IN}	Input Capacitance	5	pF	$V_{IN} = 0$ V
C_{OUT}	Output Capacitance	6	pF	$V_{OUT} = 0$ V

Effective capacitance calculated from the equation

$C = \frac{\Delta Q}{\Delta V}$ where $\Delta V = 3$ V.

Truth Table

Mode	$\overline{E}$	$\overline{W}$	D	Q	Power Level
Standby	H	X	X	HIGH Z	Standby
Read	L	H	X	D	Active
Write	L	L	D	HIGH Z	Active

HIGH Z = High impedance
D = Valid data bit
X = Don't care

Figure 1 Output Load

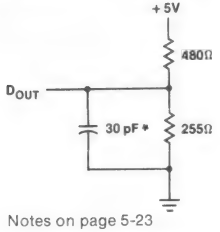
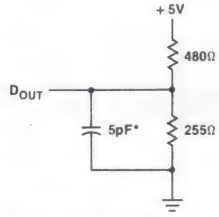


Figure 2 Output Load (for t_{EHQZ}, t_{ELQX}, t_{WLQZ}, t_{WHQX})



*Including scope and jig.

Notes on page 5-23

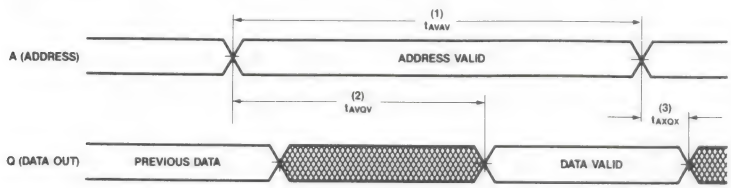
AC Operating Conditions and Characteristics: Read Cycle $T_C = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 10\%$

No.	Symbol		Parameter	F1601-45		F1601-55		F1601-70		Unit	Notes
	Standard	Alternate		Min	Max	Min	Max	Min	Max		
1	t_{AVAV}	t_{RC}	Address Valid to Address Valid (Read Cycle Time)	45		55		70		ns	5,6,9
2	t_{AVQV}	t_{AA}	Address Valid to Output Valid (Address Access Time)		45		55		70	ns	5
3	t_{AXQX}	t_{OH}	Address Invalid to Output Invalid (Output Hold Time)	5		5		5		ns	
4	t_{ELEH}	t_{RC}	Chip Enable LOW to Chip Enable HIGH (Read Cycle Time)	45		55		70		ns	6,9
5	t_{ELQV}	t_{ACS}	Chip Enable LOW to Output Valid (Chip Enable Access Time)		45		55		70	ns	6
6	t_{ELQX}	t_{LZ}	Chip Enable LOW to Output Invalid (Chip Enable to Output Active)	0		0		0		ns	4
7	t_{EHQZ}	t_{HZ}	Chip Enable HIGH to Output High Z (Chip Disable to Output Disable)	0	20	0	25	0	30	ns	4, 10
8	t_{ELICCH}	t_{PU}	Chip Enable LOW to Power Up	0		0		0		ns	4
9	t_{EHICCL}	t_{PD}	Chip Enable HIGH to Power Down		40		40		40	ns	4

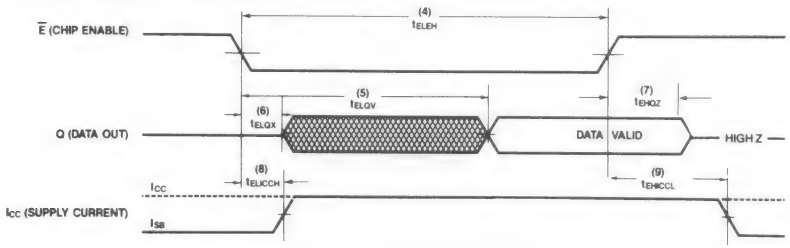
Notes on page 5-23

Timing Waveforms

Read Cycle 1 (Where $\overline{E}$ is active prior to address change. $\overline{W}$ = HIGH)



Read Cycle 2 (Where address is valid prior to $\overline{E}$ becoming active. $\overline{W}$ = HIGH)

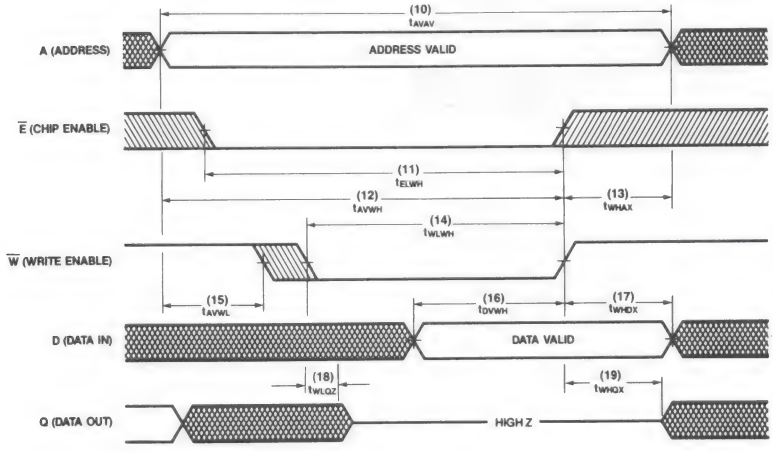


AC Operating Conditions and Characteristics: Write Cycle 1 $T_C = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 10\%$

No.	Symbol		Parameter	F1601-45		F1601-55		F1601-70		Unit	Notes
	Standard	Alternate		Min	Max	Min	Max	Min	Max		
10	t_{AVAV}	t_{WC}	Address Valid to Address Valid (Write Cycle Time)	45		55		70		ns	7,8,9
11	t_{ELWH}	t_{CW}	Chip Enable to Write HIGH (Chip Enable to End of Write)	40		45		55		ns	11
12	t_{AVWH}	t_{AW}	Address Valid to Write HIGH (Address Setup to End of Write)	40		45		55		ns	11
13	t_{WHAX}	t_{WR}	Write HIGH to Address Don't Care (Address Hold After End of Write)	0		0		0		ns	11
14	t_{WLWH}	t_{WP}	Write LOW to Write HIGH (Write Pulse Width)	20		25		40		ns	11
15	t_{AVWL}	t_{AS}	Address Valid to Write LOW (Address Setup to Beginning of Write)	5		5		5		ns	11
16	t_{DVWH}	t_{DW}	Data Valid to Write HIGH (Data Setup to End of Write)	15		20		30		ns	11
17	t_{WHDX}	t_{DH}	Write HIGH to Data Don't Care (Data Hold After End of Write)	0		0		0		ns	11
18	t_{WLQZ}	t_{WZ}	Write LOW to Output High Z (Write Enable to Output Disable)	0	20	0	25	0	30	ns	4, 10
19	t_{WHQX}	t_{OW}	Write HIGH to Output Don't Care (Output Active After End of Write)	0		0		0		ns	4

Notes on page 5-23

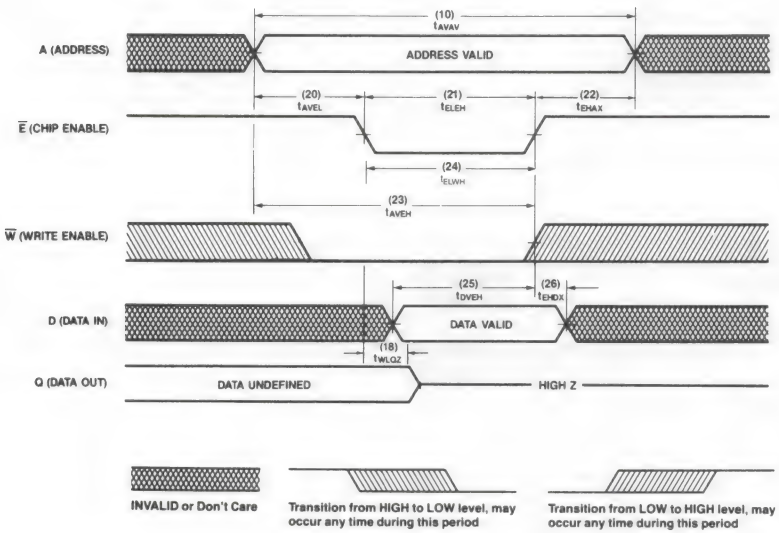
Write Cycle 1 ($\overline{W}$ controlled, where $\overline{E}$ is active prior to $\overline{W}$ becoming active.)



AC Operating Conditions and Characteristics: Write Cycle $T_C = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 10\%$

No.	Symbol		Parameter	F1601-45		F1601-55		F1601-70		Unit	Notes
	Standard	Alternate		Min	Max	Min	Max	Min	Max		
20	t_{AVEL}	t_{AS}	Address Valid to Chip Enable LOW (Address Set UP)	0		0		0		ns	
21	t_{ELEH}	t_{CW}	Chip Enable LOW to Chip Enable HIGH (Write Cycle Time)	45		55		70		ns	11
22	t_{EHAX}	t_{WR}	Chip Enable HIGH to Address Don't Care (Address Hold After End of Write)	0		0		0		ns	
23	t_{AVEH}	t_{AW}	Address Valid to Chip Enable HIGH (Address Setup to End of Write)	40		45		55		ns	
24	t_{ELWH}	t_{WP}	Chip Enable LOW to Write HIGH (Write Pulse Width)	30		35		40		ns	11
25	t_{DVEH}	t_{DW}	Data Valid to Chip Enable HIGH (Data Setup to End of Write)	15		20		30		ns	
26	t_{EHDX}	t_{DH}	Chip Enable HIGH to Data Don't Care (Data Hold)	0		0		0		ns	

Write Cycle 2 ($\overline{E}$ controlled, where $\overline{W}$ is active prior to $\overline{E}$ becoming active. *See Note 9.*)

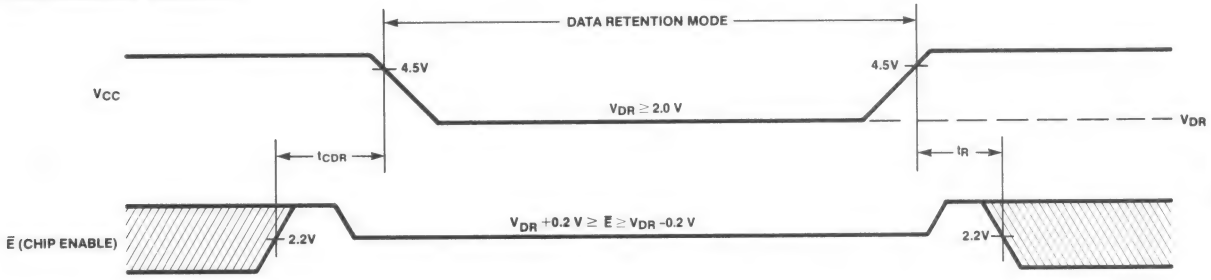


Notes on page 5-23

Data Retention Characteristics: $T_C = 0°C$ to $+70°C$, $V_{CC} = 3.0V$ to $5.5V$

Symbol	Parameter	Conditions		Min.	Max.	Unit	Notes
V_{DR}	V_{CC} Voltage for Data Retention	$V_{CC} - 0.2\ V \le \overline{E} \le V_{CC} + 0.5$ $V_{CC} - 0.2\ V \le V_{IN} \le V_{CC} + 0.5\ V$ or $V_{SS} - 0.5\ V \le V_{IN} \le V_{SS} + 0.5\ V$		2.0	5.5	V	
I_{CCDR}	Data Retention Current	$V_{DR} = 3.0\ V$	$T_C = 0°C$ to $+70°C$		50	μA	15
t_{CDR}	Chip Disable to Data Retention Time			0		ns	
t_R	Recovery Time			t_{AVAV}		ns	14

Data Retention Waveform



Notes

1. This parameter is measured with $\overline{E}$ HIGH (chip deselected) and inputs at valid TTL levels.
2. This parameter is measured with Address, $\overline{W}$ and D inputs all satisfying one of two conditions: $V_{CC} - 0.2\ V \le V_{IN} \le V_{CC} + 0.5\ V$ or $V_{SS} - 0.5\ V \le V_{IN} \le V_{SS} + 0.2\ V$. In addition, the Enable input must be $V_{CC} - 0.2\ V \le \overline{E} \le V_{CC} + 0.5\ V$. This condition results in significant reduction in current in the input buffer circuitry and consequently a lower overall current level.
3. Operation to specifications guaranteed 2.0 ms after V_{CC} applied.
4. This parameter is sampled and not 100% tested.
5. Read Cycle 1 assumes that Chip Enable ($\overline{E}$) occurs before the addresses are valid. Timing considerations are referenced to the edges of Address Valid.
6. Read Cycle 2 assumes that Address Valid occurs prior to Chip Enable ($\overline{E}$). Timing considerations are referenced to the edges of Chip Enable.
7. Since a write cycle can only occur during intervals where both $\overline{E}$ and $\overline{W}$ are LOW, Write Cycle 1 assumes that W is the latter of the two signals to go LOW (active) and is also the first of the two signals to go HIGH (inactive). Consequently, timing considerations are referenced to the edges of $\overline{W}$ rather than $\overline{E}$.
8. Write Cycle 2 assumes that, of the two control signals, $\overline{E}$ and $\overline{W}$, $\overline{E}$ is the latter of the two to go LOW (active) and is also the first of the two to go HIGH (inactive). Consequently, timing considerations are referenced to the edges of $\overline{E}$ rather than $\overline{W}$.
9. All READ and WRITE cycle timings are referenced from the last bit to become valid address to the first transitioning address.
10. Transition to high impedance state to measured ±500 mV from steady state voltage with specified loading in *Figure 2*. This parameter is sampled not 100% tested.
11. Since Write Enable ($\overline{W}$) is gated internally with Chip Enable ($\overline{E}$), the value of $\overline{W}$ during periods where $\overline{E}$ is HIGH is irrelevant (i.e., don't care). Thus whenever $\overline{W}$ transitions to the LOW state piror to $\overline{E}$, all timing references will be to the falling edge of $\overline{E}$ rather than W. Similarly, whenever $\overline{E}$ transitions to the HIGH state prior to $\overline{W}$, all timing references will be to the rising edge of $\overline{E}$ rather than $\overline{W}$.
12. Input pulse levels 0 to 3.0 Volts.
13. Input rise and fall times are assumed to be 5 ns. Timing measurement reference levels are 1.5 Volts.
14. T_{AVAV} = Read Cycle Timing.
15. $V_{cc} - 0.2\ V \le \overline{E} \le V_{cc} + 0.5\ V$. $V_{cc} - 0.2\ V \le V_{in} \le V_{cc} + 0.5V$ or $V_{ss} - 0.5\ V \le V_{in} \le V_{ss} + 0.5\ V$
16. Rise and fall times should not exceed 45 ns.

Ordering Information

Part Number	Access Time	Temperature Range	Package	Order Code
F1601-45	45 ns	0°C to + 70°C	Side-brazed	1601DC45
F1601-45	45 ns	0°C to + 70°C	Leadless Chip Carrier	1601LC45
F1601-45	45 ns	0°C to + 70°C	Plastic DIP	1601PC45
F1601-55	55 ns	0°C to + 70°C	Side-brazed	1601DC55
F1601-55	55 ns	0°C to + 70°C	Leadless Chip Carrier	1601LC55
F1601-55	55 ns	0°C to + 70°C	Plastic DIP	1601PC55
F1601-70	70 ns	0°C to + 70°C	Side-brazed	1601DC70
F1601-70	70 ns	0°C to + 70°C	Leadless Chip Carrier	1601LC70
F1601-70	70 ns	0°C to + 70°C	Plastic DIP	1601PC70

FAIRCHILD
A Schlumberger Company

F1601
65,536 x 1-Bit Static RAM
Data Retention Version
Military Temperature Range

Memory & High Speed Logic

Description

The F1601 is a 65,536-bit fully static asynchronous random access memory, organized as 65,536 words by 1-bit, using high-performance CMOS technology. The F1601 is based on an advanced isoplanar oxide isolation process: fully-implanted CMOS technology with sub-2 micron design rules and high-performance tantalum silicide gate electrodes. The high-density NMOS memory array and the CMOS peripheral circuits provide fast access time plus low active and standby power.

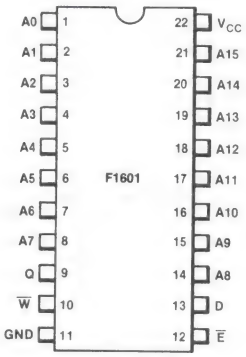
- **Single +5V Operation (±10%)**
- **Fast Access Time: 55 ns/70 ns (Maximum)**
- **Power Dissipation (Normal Operation):**
  - **70 mA Maximum (Active)**
  - **20 mA Maximum (Standby — TTL Input Levels)**
  - **9 mA Maximum (Standby — CMOS Input Levels)**
- **Data Retention Supply Voltage**
  - **2.0V to 5.5V**
- **Low Power Dissipation (Data Retention)**
  - **I_{CCDR} = 200 μA Maximum (V_{DR} = 2.0V)**
  - **I_{CCDR} = 400 μA Maximum (V_{DR} = 3.0V)**
- **Fully Static: No Clock or Timing Strobe Required**
- **Specifications Guaranteed Over Full Millitary Temperature Range (-55°C to +125°C)**
- **Directly TTL Compatible — All Inputs and Outputs**
- **Separate Data Input and Three-State Output**
- **Available in a 22-Pin DIP or LCC**
- **Polyimide Die Coat for Alpha Immunity**

Pin Names

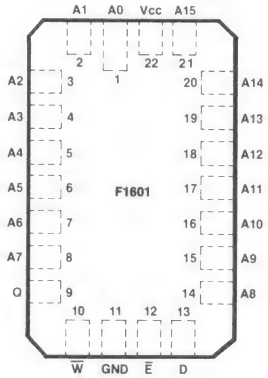
A_0-A_{15}	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output
V_{CC}	Power (5.0 V)
GND	Ground (0 V)

Connection Diagrams

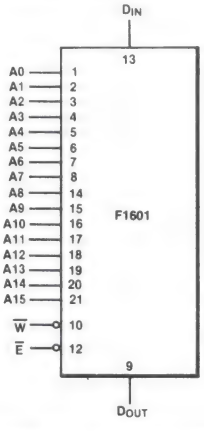
22-Pin DIP (Top View)



22-Pin LCC (Top View)



Logic Symbol



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Absolute Maximum Ratings

Voltage on Any Input or Output Pin With Respect to GND	-2.0V to 7.0V
Storage Temperature Range	-65° C to +150° C
Operating Temperature Range	-55° C to +125° C
Power Dissipation	1.0W
Maximum Junction Temperature (T_J)	+150° C
Thermal Resistance, Junction to Case (θ_{JC}): Case (Side-Brazed DIP)	15° C/W

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions: T_C = -55° C to +125° C

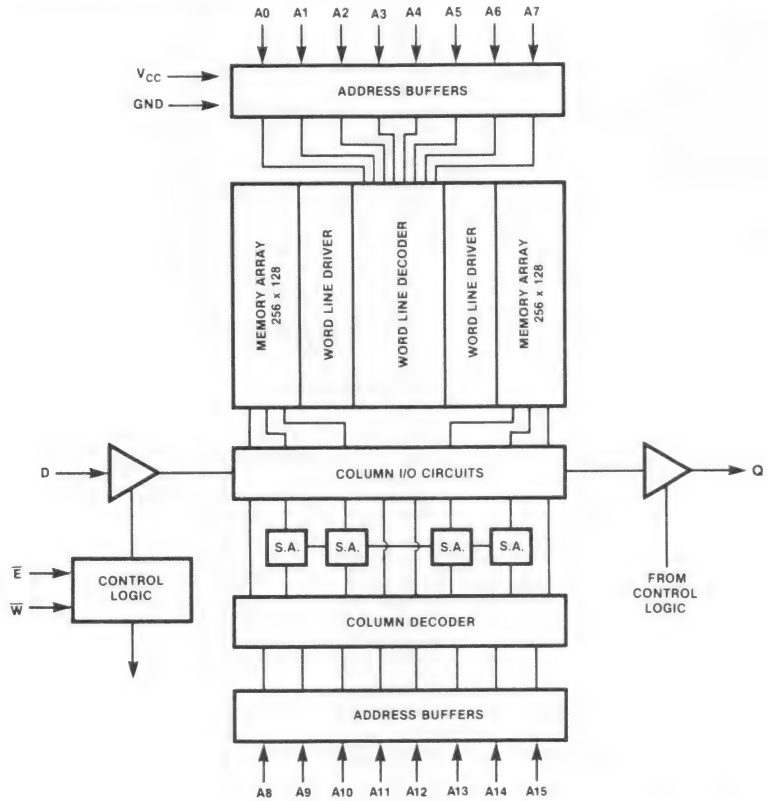
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		6.0	V
V_{IL}	Input LOW Voltage	-0.5*		0.8	V

All voltages are referenced to GND pin = 0 V.

*The device will withstand undershoots to -3.0 V of 20 ns durations. This is guaranteed by bench simulation in a DC mode, not 100% tested.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Functional Block Diagram



DC Characteristics: $T_C = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$

Symbol	Characteristic	F1601-55 Min.	F1601-55 Max.	F1601-70 Min.	F1601-70 Max.	Unit	Condition
I_{IN}	Input Leakage Current (All inputs)		±5		±5	μA	$V_{CC} = 5.5\ V$, $V_{IN} = 0\ V$ and 5.5 V
I_{OUT}	Output Leakage Current (on Q)		±10		±10	μA	$\overline{E} = V_{IH}$ $V_{OUT} = 0\ V$ and 5.5 V
I_{CC1}	Operating Power Supply Current		70		70	mA	$\overline{E} = V_{IL}$ Output Open
I_{CC2}	Dynamic Operating Supply Current		70		70	mA	Min. Read Cycle Time Duty Cycle = 100% Output Open
I_{SB1}	Standby Supply Current		20		20	mA	$\overline{E} \geq V_{IH}$, see *note 1*
I_{SB2}	Full Standby Supply Current		9.0		9.0	mA	*see note 2*
I_{OS}	Output Current Short Circuit to Ground		-135		-135	mA	$V_{CC} = 5.5\ V$ Duration not to Exceed 1 Second
V_{OL}	Output LOW Voltage		0.4		0.4	V	$I_{OL} = 8.0\ mA$
V_{OH}	Output HIGH Voltage	2.4		2.4		V	$I_{OH} = -4.0\ mA$

AC Test Conditions[3]

Input Pulse Levels ..... GND to 3.0 V
Input Rise and Fall Times ..... 5 ns
Input and Output Timing Reference Levels ..... 1.5 V
Output Load ..... *See Figures 1 and 2*

Capacitance[4]: $T_C = +25°C$, $f = 1.0\ MHz$

Symbol	Parameter	Max.	Units	Conditions
C_{IN}	Input Capacitance	5	pF	$V_{IN} = 0\ V$
C_{OUT}	Output Capacitance	6	pF	$V_{OUT} = 0\ V$

Effective capacitance calculated from the equation

$C = \frac{\Delta Q}{\Delta V}$ where $\Delta V = 3\ V$.

Truth Table[5]

Mode	$\overline{E}$	$\overline{W}$	D	Q	Power Level
Standby	H	X	X	HIGH Z	Standby
Read	L	H	X	D	Active
Write	L	L	D	HIGH Z	Active

HIGH Z = High impedance
D = Valid data bit
X = Don't care

Figure 1 Output Load

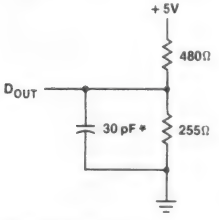
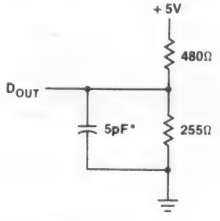


Figure 2 Output Load (for t_{EHQZ}, t_{ELQX}, t_{WLQZ}, t_{WHQX})



*Including scope and jig.

Notes on page 5-31

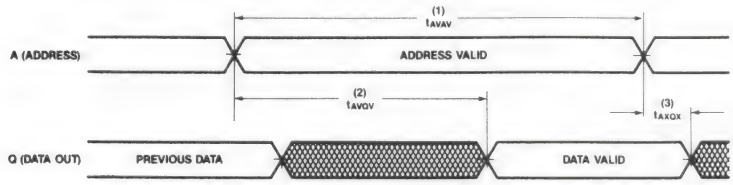
AC Operating Conditions and Characteristics: Read Cycle T_C = -55° C to +125° C, V_{CC} = 5.0V ±10%

No.	Symbol		Parameter	F1601-55		F1601-70		Unit	Notes
	Standard	Alternate		Min.	Max.	Min.	Max.		
1	t_{AVAV}	t_{RC}	Address Valid to Address Valid (Read Cycle Time)	55		70		ns	6,7,10
2	t_{AVQV}	t_{AA}	Address Valid to Output Valid (Address Access Time)		55		70	ns	6
3	t_{AXQX}	t_{OH}	Address Invalid to Output Invalid (Output Hold Time)	5		5		ns	
4	t_{ELEH}	t_{RC}	Chip Enable LOW to Chip Enable HIGH (Read Cycle Time)	55		70		ns	7,10
5	t_{ELQV}	t_{ACS}	Chip Enable LOW to Output Valid (Chip Enable Access Time)		55		70	ns	7
6	t_{ELQX}	t_{LZ}	Chip Enable LOW to Output Invalid (Chip Enable to Output Active)	0		0		ns	4
7	t_{EHQZ}	t_{HZ}	Chip Enable HIGH to Output High Z (Chip Disable to Output Disable)	0	35	0	40	ns	4,11
8	t_{ELICCH}	t_{PU}	Chip Enable LOW to Power Up	0		0		ns	4
9	t_{EHICCL}	t_{PD}	Chip Enable HIGH to Power Down		45		45	ns	4

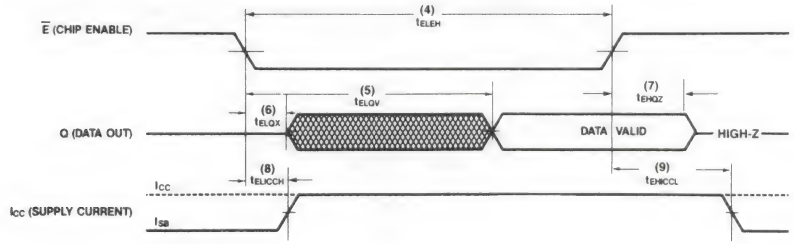
Notes on page 5-31

Timing Waveforms

Read Cycle 1 (Where $\overline{E}$ is active prior to address change. $\overline{W}$ = HIGH)



Read Cycle 2 (Where address is valid prior to $\overline{E}$ becoming active. $\overline{W}$ = HIGH)

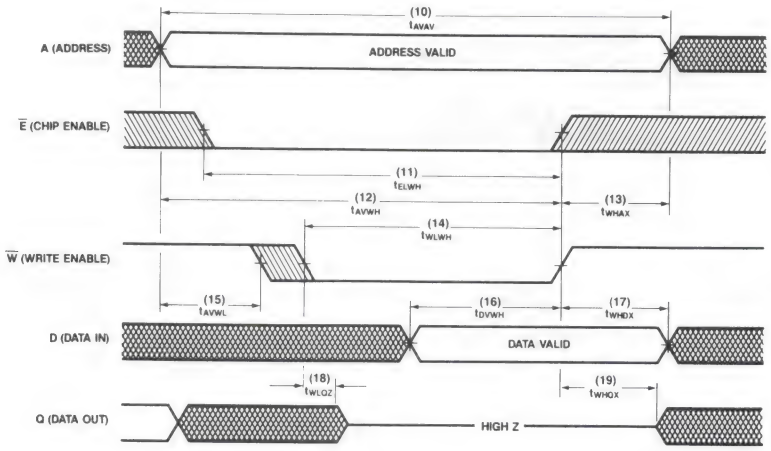


AC Operating Conditions and Characteristics: Write Cycle 1 T_C = -55° C to +125° C, V_{CC} = 5.0 V ±10%

No.	Symbol		Parameter	F1601-55		F1601-70		Unit	Notes
	Standard	Alternate		Min.	Max.	Min.	Max.		
10	t_{AVAV}	t_{WC}	Address Valid to Address Valid (Write Cycle Time)	55		70		ns	8,9,10
11	t_{ELWH}	t_{CW}	Chip Enable to Write HIGH (Chip Enable to End of Write)	50		55		ns	12
12	t_{AVWH}	t_{AW}	Address Valid to Write HIGH (Address Setup to End of Write)	50		55		ns	12
13	t_{WHAX}	t_{WR}	Write HIGH to Address Don't Care (Address Hold After End of Write)	5		5		ns	12
14	t_{WLWH}	t_{WP}	Write LOW to Write HIGH (Write Pulse Width)	35		40		ns	12
15	t_{AVWL}	t_{AS}	Address Valid to Write LOW (Address Setup to Beginning of Write)	15		15		ns	12
16	t_{DVWH}	t_{DW}	Data Valid to Write HIGH (Data Setup to End of Write)	25		30		ns	12
17	t_{WHDX}	t_{DH}	Write HIGH to Data Don't Care (Data Hold After End of Write)	5		5		ns	12
18	t_{WLQZ}	t_{WZ}	Write LOW to Output High Z (Write Enable to Output Disable)	0	30	0	35	ns	4,11
19	t_{WHQZ}	t_{OW}	Write HIGH to Output Don't Care (Output Active After End of Write)	0		0		ns	4

Notes on page 5-31

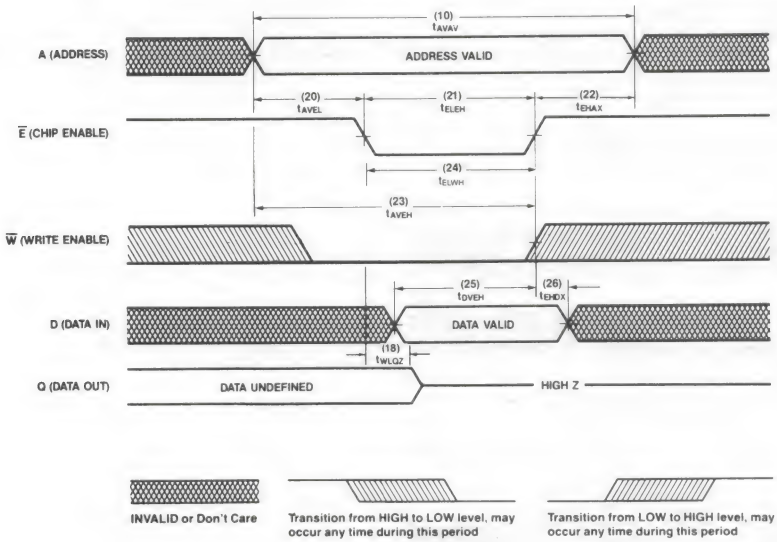
Write Cycle 1 ($\overline{W}$ controlled, where $\overline{E}$ is active prior to $\overline{W}$ becoming active.)



AC Operating Conditions and Characteristics: Write Cycle 2 $T_C = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$

No.	Symbol		Parameter	F1601-55		F1601-70		Unit	Notes
	Standard	Alternate		Min.	Max.	Min.	Max.		
20	t_{AVEL}	t_{AS}	Address Valid to Chip Enable LOW (Address Set Up)	5		5		ns	
21	t_{ELEH}	t_{CW}	Chip Enable LOW to Chip Enable HIGH (Write Cycle Time)	55		70		ns	12
22	t_{EHAX}	t_{WR}	Chip Enable HIGH to Address Don't Care (Address Hold After End of Write)	5		5		ns	
23	t_{AVEH}	t_{AW}	Address Valid to Chip Enable HIGH (Address Setup to End of Write)	50		65		ns	
24	t_{ELWH}	t_{WP}	Chip Enable LOW to Write HIGH (Write Pulse Width)	35		40		ns	12
25	t_{DVEH}	t_{DW}	Data Valid to Chip Enable HIGH (Data Setup to End of Write)	25		30		ns	
26	t_{EHDX}	t_{DH}	Chip Enable HIGH to Data Don't Care (Data Hold)	5		5		ns	

Write Cycle 2 ($\overline{E}$ controlled, where $\overline{W}$ is active prior to $\overline{E}$ becoming active. *See Note 9.*)

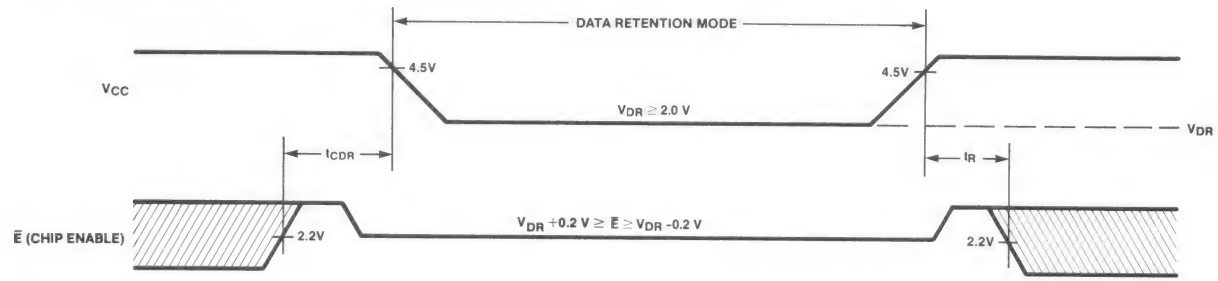


Notes on page 5-31

Data Retention Characteristics: T_C = -55° C to +125° C, V_{CC} = 2.0V to 5.5V

Symbol	Parameter	Conditions		Min.	Max.	Unit	Notes
V_{DR}	V_{CC} Voltage for Data Retention	V_{CC} - 0.2 V ≤ $\overline{E}$ ≤ V_{CC} + 0.5 V_{CC} -0.2 V ≤ V_{IN} ≤ V_{CC} +0.5 V or V_{SS} -0.2V ≤ V_{IN} ≤ V_{SS} +0.5 V		2.0	5.5	V	
I_{CCDR}	Data Retention Current	V_{DR} = 2.0 V	T_C = -55° C and +25° C		5	µA	16
			T_C = +125° C		200	µA	16
		V_{DR} = 3.0 V	T_C = -55° C and +25° C		8	µA	16
			T_C = +125° C		400	µA	16
t_{CDR}	Chip Disable to Data Retention Time			0		ns	
t_R	Recovery Time			t_{AVAV}		ns	15

Data Retention Waveform



Notes

1. This parameter is measured with Chip Enable ($\overline{E}$) HIGH and inputs at valid TTL levels (0.8V and 2.2V).
2. This parameter is measured with Address, $\overline{W}$ and D inputs all satisfying one of two conditions: V_{CC} -0.2 V ≤ V_{IN} ≤ V_{CC} +0.5 V or V_{SS} -0.5 V ≤ V_{IN} ≤ V_{SS} +0.2 V. In addition, the Enable input must be V_{CC} -0.2 V ≤ $\overline{E}$ ≤ V_{CC} +0.5 V. This condition results in significant reduction in current in the input buffer circuitry and consequently a lower overall current level.
3. Operation to specifications guaranteed 2.0 ms after V_{CC} applied.
4. This parameter is based on initial design qualification and is also verified on every design change. These are not tested in production.
5. Functional test performed with the following input conditions: V_{IL} = 0.4 V and V_{IH} = 2.4 V.
6. Read Cycle 1 assumes that Chip Enable ($\overline{E}$) occurs before the addresses are valid. Timing considerations are referenced to the edges of Address Valid.
7. Read Cycle 2 assumes that Address Valid occurs prior to Chip Enable ($\overline{E}$). Timing considerations are referenced to the edges of Chip Enable.
8. Since a write cycle can only occur during intervals where both $\overline{E}$ and $\overline{W}$ are LOW, Write Cycle 1 assumes that W is the latter of the two signals to go LOW (active) and is also the first of the two signals to go HIGH (inactive). Consequently, timing considerations are referenced to the edges of $\overline{W}$ rather than $\overline{E}$.
9. Write Cycle 2 assumes that, of the two control signals, $\overline{E}$ and $\overline{W}$. $\overline{E}$ is the latter of the two to go LOW (active) and is also the first of the two to go HIGH (inactive). Consequently, timing considerations are referenced to the edges of $\overline{E}$ rather than $\overline{W}$.
10. All READ and WRITE cycle timings are referenced from the last bit to become valid address to the first transitioning address.
11. Transition to high impedance state to measured ±500 mV from steady state voltage with specified loading in *Figure 2*.
12. Since Write Enable ($\overline{W}$) is gated internally with Chip Enable ($\overline{E}$), the value of W during periods where $\overline{E}$ is HIGH is irrelevant (i.e., don't care). Thus whenever $\overline{W}$ transitions to the LOW state prior to $\overline{E}$, all timing references will be to the falling edge of $\overline{E}$ rather than $\overline{W}$. Similarly, whenever $\overline{E}$ transitions to the HIGH state prior to $\overline{W}$, all timing references will be to the rising edge of $\overline{E}$ rather than $\overline{W}$.
13. Input pulse levels 0 to 3.0 Volts.
14. Input rise and fall times are assumed to be 5 ns. Timing measurement reference levels are 1.5 Volts.
15. T_{AVAV} = Read Cycle Timing.
16. V_{CC} -0.2 V ≤ $\overline{E}$ ≤ V_{CC} +0.5 V. V_{CC} -0.2 V ≤ V_{IN} ≤ V_{CC} + 0.5 V or -0.5V ≤ V_{IN} ≤ 0.2 V.
17. Rise and fall times should not exceed 45 ns.

Ordering Information

Part Number	Access Time	Temperature Range	Package	Order Code
F1601-55	55 ns	- 55° to +125°C	Side-brazed	1601DMQB55
F1601-55	55 ns	- 55° to +125°C	Leadless Chip Carrier	1601LMQB55
F1601-70	70 ns	- 55° to +125°C	Side-brazed	1601DMQB70
F1601-70	70 ns	- 55° to +125°C	Leadless Chip Carrier	1601LMQB70

FAIRCHILD
A Schlumberger Company

F1620
16,384 x 4-Bit Static RAM

Memory and High Speed Logic

Description

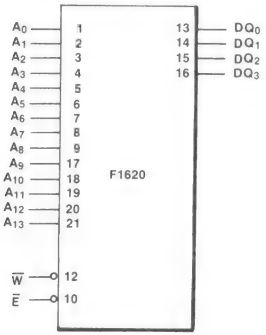
The F1620 is a 65,536-bit fully static asynchronous random access memory, organized as 16,384 words by 4-bits per word, using high-performance CMOS technology. The F1620 is based on an advanced isoplanar oxide isolation process: fully-implanted CMOS technology with sub-2 micron design rules and high-performance tantalum silicide gate electrodes. The high-density NMOS memory array and the CMOS peripheral circuits provide fast access time plus low active and standby power.

- **Single +5V Operation (±10%)**
- **Fully Static: No Clock or Timing Strobe Required**
- **Fast Access Time:**
  - **Commercial: 25 ns/35 ns (Maximum)**
  - **Military: 35 ns/45 ns (Maximum)**
- **Available in Commercial (0°C to +70°C) or Military (-55°C to +125°C) Versions**
- **Low Power Dissipation:**
  - **90/70 mA Maximum (Active)**
  - **20/15 mA Maximum (Standby — TTL Input Levels)**
  - **2 mA Maximum (Standby — CMOS Input Levels)**
- **Directly TTL Compatible — All Inputs and Outputs**
- **Available in a 22-Pin DIP or 22-Terminal LCC**
- **Polyimide Die Coat for Alpha Immunity**

Pin Names

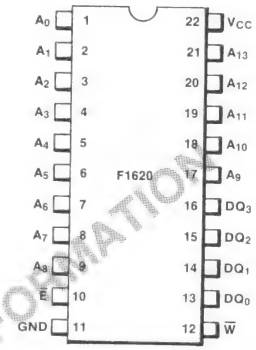
A_0-A_{13}	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
DQ_0-DQ_3	Data Inputs/Outputs
V_{CC}	Power (5.0 V)
GND	Ground (0 V)

Logic Symbol

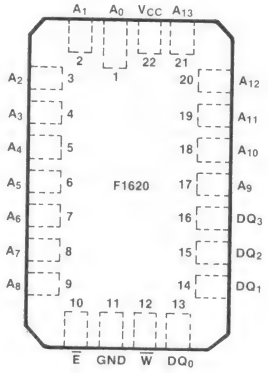


Connection Diagrams

22-Pin DIP (Top View)



22-Pin LCC (Top View)



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FAIRCHILD
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F1621
16,384 x 4-Bit Static RAM
Data Retention Version

Memory and High Speed Logic

Description

The F1621 is a 65,536-bit fully static asynchronous random access memory, organized as 16,384 words x 4-bits per word, using high-performance CMOS technology. The F1621 is based on an advanced isoplanar oxide isolation process: fully-implanted CMOS technology with sub-2 micron design rules and high-performance tantalum silicide gate electrodes. The high-density NMOS memory array and the CMOS peripheral circuits provide fast access time plus low active and standby power. The F1621 offers data retention when backed up by 2V.

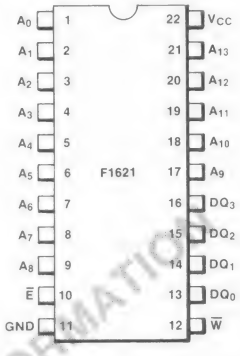
- **Single +5V Operation (±10%)**
- **Fast Access Time:**
  Commercial: 25 ns/35 ns (Maximum)
  Military: 35 ns/45 ns (Maximum)
- **Available in Commercial (0°C to +70°C) or Military (-55°C to +125°C) Versions**
- **Power Dissipation (Normal Operation):**
  90/70 mA Maximum (Active)
  20/15 mA Maximum (Standby — TTL Input Level)
  2 mA Maximum (Standby — CMOS Input Levels)
- **Data Retention Supply Voltage**
  2.0V to 5.5V
- **Low Power Dissipation (Data Retention -Commercial)**
  I_{CCDR} = 50 μA Maximum (2.0 V ≤ V_{DR} ≤ 3.0V)
- **Low Power Dissipation (Data Retention - Military)**
  I_{CCDR} = 200 μA Maximum (V_{DR} = 2.0V)
  I_{CCDR} = 400 μA Maximum (V_{DR} = 3.0V)
- **Fully Static: No Clock or Timing Strobe Required**
- **Directly TTL Compatible — All Inputs and Outputs**
- **Available in a 22-Pin DIP or 22-Terminal LCC**
- **Polyimide Die Coat for Alpha Immunity**

Pin Names

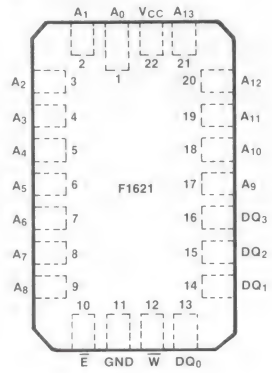
A_0-A_{13}	Address Inputs
$\overline{E}$	Chip Write Enable
$\overline{W}$	Write Enable
DQ_0-DQ_3	Data Inputs/Outputs
V_{CC}	Power (5.0V)
GND	Ground (0V)

Connection Diagrams

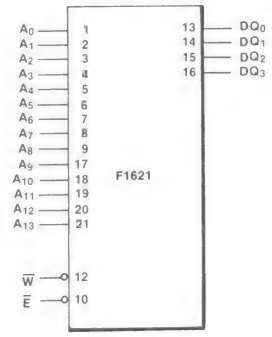
22-Pin DIP (Top View)



22-Pin LCC(Top View)



Logic Symbol



FAIRCHILD
A Schlumberger Company

F1622
16,384 x 4-Bit Static RAM

Memory and High Speed Logic

Description

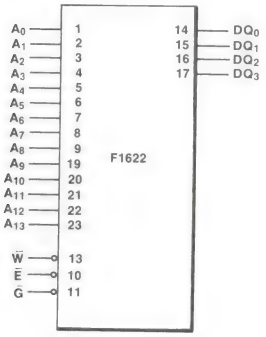
The F1622 is a 65,536-bit fully static asynchronous random access memory, organized as 16,384 words by 4-bits per word, using high-performance CMOS technology. The F1622 is based on an advanced isoplanar oxide isolation process: fully-implanted CMOS technology with sub-2 micron design rules and high-performance tantalum silicide gate electrodes. The high-density NMOS memory array and the CMOS peripheral circuits provide fast access time plus low active and standby power.

- **Single +5V Operation (±10%)**
- **Fully Static: No Clock or Timing Strobe Required**
- **Fast Access Time:**
  Commercial: 25 ns/35 ns (Maximum)
  Military: 35 ns/45 ns (Maximum)
- **Available in Commercial (0°C to +70°C) or Military (-55°C to +125°C) Versions**
- **Low Power Dissipation:**
  90/70 mA Maximum (Active)
  20/15 mA Maximum (Standby — TTL Input Levels)
  2 mA Maximum (Standby — CMOS Input Levels)
- **Directly TTL Compatible — All Inputs and Outputs**
- **Available in a 24-Pin DIP or 28-Terminal LCC**
- **Polyimide Die Coat for Alpha Immunity**

Pin Names

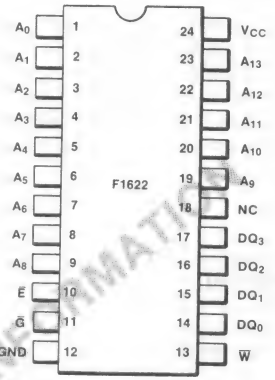
A_0-A_{13}	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ_0-DQ_3	Data Inputs/Outputs
V_{CC}	Power (5.0V)
GND	Ground (0V)
NC	No Connection

Logic Symbol

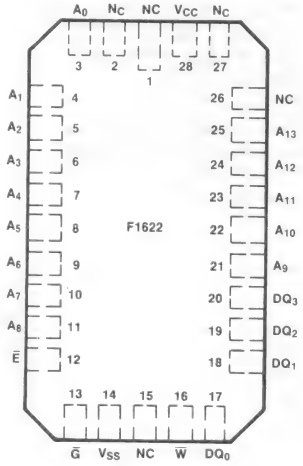


Connection Diagrams

24-Pin DIP (Top View)



28-Pin LCC (Top View)



5

FAIRCHILD
A Schlumberger Company

F1623
16,384 x 4-Bit Static RAM
Data Retention Version

Memory and High Speed Logic

Description

The F1623 is a 65,536-bit fully asynchronous random access memory, organized as 16,384 words by 4-bits per word, using high-performance CMOS technology. The F1623 is based on an advanced isoplanar oxide isolation process: fully-implanted CMOS technology with sub-2 micron design rules and high-performance tantalum silicide gate electrodes. The high-density NMOS memory array and the CMOS peripheral circuits provide fast access time plus low active and standby power. The F1623 offers data retention when backed up by 2V.

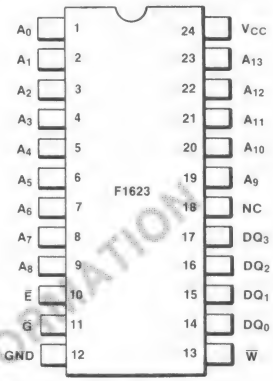
- **Single +5V Operation (±10%)**
- **Fast Access Time:**
  Commercial: 25 ns/35 ns (Maximum)
  Military: 35 ns/45 ns (Maximum)
- **Available in Commercial (0°C to 70°C) or Military (-55°C to +125°C) Versions**
- **Power Dissipation (Normal Operation):**
  90/70 mA Maximum (Active)
  20/15 mA Maximum (Standby — TTL Input Levels)
  2 mA Maximum (Standby — CMOS Input Levels)
- **Data Retention Supply Voltage**
  2.0V to 5.5V
- **Low Power Dissipation (Data Retention-Commercial)**
  I_{CCDR} = 50 μA Maximum (2.0V ≤ V_{DR} ≤ 3.0V)
- **Low Power Dissipation (Data Retention-Military)**
  I_{CCDR} = 200 μA Maximum (V_{DR} =2.0V)
  I_{CCDR} = 400 μA Maximum (V_{DR} = 3.0V)
- **Fully Static: No Clock or Timing Strobe Required**
- **Directly TTL Compatible — All inputs and Outputs**
- **Available in a 24-Pin DIP or 28-Terminal LCC**
- **Polyimide Die Coat for Alpha Immunity**

Pin Names

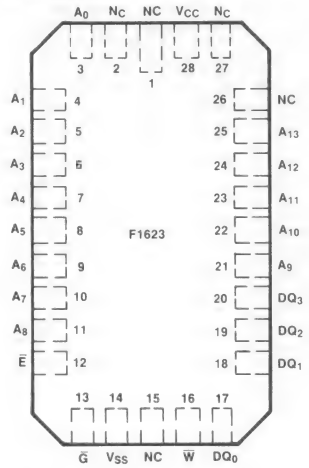
A_0-A_{13}	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ_0-DQ_3	Data Inputs/Outputs
V_{CC}	Power (5.0V)
GND	Ground (0V)
NC	No Connection

Connection Diagrams

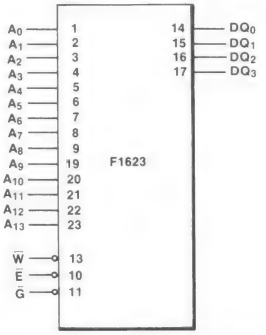
24-Pin DIP (Top View)



28-Pin LCC (Top View)



Logic Symbol



Notes

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F100K DC Family Specifications

DC characteristics for the F100K series family parametric limits listed below are guaranteed for the entire F100K ECL family unless specified on the individual data sheet.

Absolute Maximum Ratings: Above which the useful life may be impaired[1]

Storage Temperature	−65° C to +150° C
Maximum Junction Temperature (T_J)	+175° C
Supply Voltage Range	−7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	−50 mA
Operating Range[2]	−5.7 V to −4.2 V
Lead Temperature (Soldering 10 sec)	300° C

DC Performance Characteristics: V_{EE} = −4.5 V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, Note 3

Symbol	Characteristic	Min	Max	Unit	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−880	mV	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	Loading with 50 Ω to −2.0 V
V_{OL}	Output LOW Voltage	−1810	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035		mv	V_{IN} = $V_{IH(min)}$ or $V_{IL(max)}$	
V_{OLC}	Output LOW Voltage		−1610	mV		
V_{IH}	Input HIGH Voltage	−1165	−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		μA	V_{IN} = $V_{IL(min)}$	

1. Unless specified otherwise on individual data sheet.
2. Parametric values specified at −4.8 V to −4.2 V.
3. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

DC Performance Characteristics: $V_{EE} = -4.2$ V, $V_{CC} = V_{CCA} = GND$, $T_C = 0°C$ to $+85°C$, Note 3

Symbol	Characteristic	Min	Max	Unit	Conditions	
V_{OH}	Output HIGH Voltage	−1020	−870	mV	$V_{IN} = V_{IH(max)}$ or $V_{IL(min)}$	Loading with 50 Ω to −2.0 V
V_{OL}	Output LOW Voltage	−1810	−1605	mV		
V_{OHC}	Output HIGH Voltage	−1030		mv	$V_{IN} = V_{IH(min)}$ or $V_{IL(max)}$	
V_{OLC}	Output LOW Voltage		−1595	mV		
V_{IH}	Input HIGH Voltage	−1150	−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		μA	$V_{IN} = V_{IL(min)}$	

DC Performance Characteristics: $V_{EE} = -4.8$ V, $V_{CC} = V_{CCA} = GND$, $T_C = 0°C$ to $+85°C$, Note 3

Symbol	Characteristic	Min	Max	Unit	Conditions	
V_{OH}	Output HIGH Voltage	−1035	−880	mV	$V_{IN} = V_{IH(max)}$ or $V_{IL(min)}$	Loading with 50 Ω to −2.0 V
V_{OL}	Output LOW Voltage	−1830	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1045		mv	$V_{IN} = V_{IH(min)}$ or $V_{IL(max)}$	
V_{OLC}	Output LOW Voltage		−1610	mV		
V_{IH}	Input HIGH Voltage	−1165	−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810	−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		μA	$V_{IN} = V_{IL(min)}$	

Notes on preceding page

F10K DC Family Specifications

DC characteristics for the F10K series memories. Parametric limits listed below are guaranteed for all F10K memories, except where noted on individual data sheets.

Absolute Maximum Ratings: Above which the useful life may be impaired[2]

Storage Temperature	−65° C to +150° C
Maximum Junction Temperature (T_J)	+175° C
V_{EE} Pin Potential to Ground Pin	−7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	−30 mA to +0.1 mA
Lead Temperature (Soldering 10 sec)	300° C

Guaranteed Operating Ranges

Supply Voltage (V_{EE})			Case Temperature (T_C)
Min	Typ	Max	
−5.46 V	−5.2 V	−4.94 V	0°C to +75°C

DC Performance Characteristics: V_{EE} = -5.2 V, Output Load = 50 Ω and 30 pF to -2.0 V, T_C = 0° C to + 75° C[1]

Symbol	Characteristic	Min	Max	Unit	Tc	Conditions[2]	
V_{OH}	Output HIGH Voltage	−1000 −960 −900	−840 −810 −720	mV	0°C +25°C +75°C	$V_{IN} = V_{IH(max)}$ or $V_{IL(min)}$	Loading is 50 Ω to −2.0 V
V_{OL}	Output LOW Voltage	−1870 −1850 −1830	−1665 −1650 −1625	mV	0°C +25°C +75°C		
V_{OHC}	Output HIGH Voltage	−1020 −980 −920		mv	0°C +25°C +75°C	$V_{IN} = V_{IH(min)}$ or $V_{IL(max)}$	
V_{OLC}	Output LOW Voltage		−1645 −1630 −1605	mV	0°C +25°C +75°C		
V_{IH}	Input HIGH Voltage	−1145 −1105 −1045	−840 −810 −720	mV	0°C +25°C +75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input LOW Voltage	−1870 −1850 −1830	−1490 −1475 −1450	mV	0°C +25°C +75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IL}	Input LOW Current	0.5	170	μA	+25°C	$V_{IN} = V_{IL(min)}$	

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Unless specified otherwise on individual data sheet.

FAIRCHILD
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F100Z416
256 x 4-Bit Programmable Read Only Memory

Memory and High Speed Logic

Description

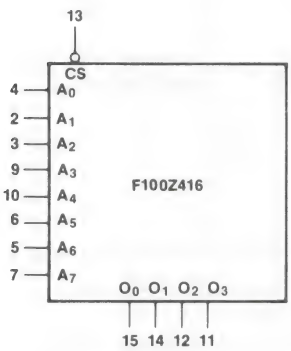
The F100Z416 is a 1024-bit field Programmable Read Only Memory (PROM), organized 256 words by four bits per word. It is designed for high-speed control, mapping, code conversion, and logic replacement. The device includes full on-chip address decoding, non-inverting Data output lines, and an active-LOW Chip Select line for easy memory expansion.

- **Address Access Time — 12 ns Typ**
- **Chip Select Input and Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{CS}$	Chip Select Input (Active LOW)
A_0–A_7	Address Inputs
O_0–O_3	Data Outputs

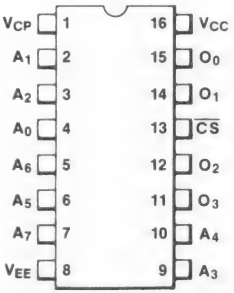
Logic Symbol



V_{CP} = Pin 1
V_{CC} = Pin 16
V_{EE} = Pin 8

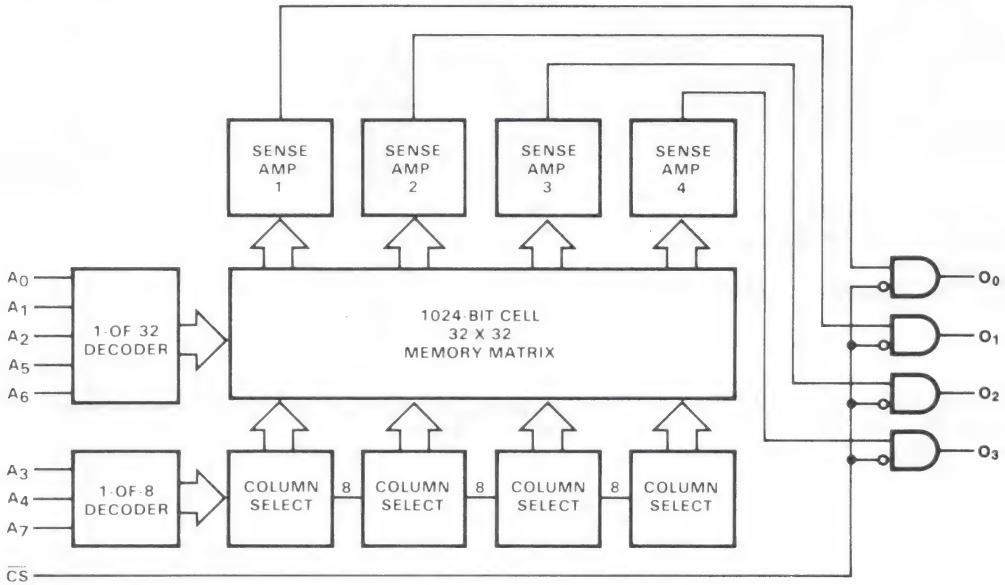
Connection Diagram

16-Pin DIP (Top View)



Note
The Flatpak version has the same pinout (Connection Diagram) as the Dual In-line Package.

Logic Diagram



Functional Description

The F100Z416 is a fully decoded bipolar field programmable read only memory organized 256 words by four bits per word. An unterminated emitter-follower output is provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many F100Z416 devices can be tied together. An external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is off.

One Chip Select ($\overline{CS}$) input is provided for memory array expansion up to 512 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of $\overline{CS}$ from the address without increasing address access time. The device is enabled when $\overline{CS}$ is LOW. When the device is disabled ($\overline{CS}$ = HIGH), all outputs are forced LOW.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the A_0 through A_7 inputs, the chip is selected and data is valid at the outputs after t_{AA}.

The F100Z416 uses open base transistor vertical (junction) fuse cells. Initially, an unprogrammed cell is in the logic '1' state. Cells can selectively be programmed to a logic '0' state by following a specified procedure which fuses aluminum through the emitter-base junction of the cell transistor.

Note: Consult factory for ordering information.

FAIRCHILD
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F10Z416
256 x 4-Bit Programmable Read Only Memory

Memory and High Speed Logic

Description

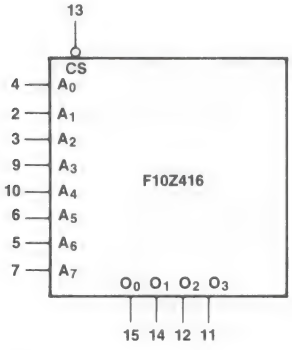
The F10Z416 is a 1024-bit field Programmable Read Only Memory (PROM), organized 256 words by four bits per word. It is designed for high-speed control, mapping, code conversion, and logic replacement. The device includes full on-chip address decoding, non-inverting Data output lines, and an active-LOW Chip Select line for easy memory expansion.

- **Address Access Time — 12 ns Typ**
- **Chip Select Input and Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{CS}$	Chip Select Input (Active LOW)
A_0–A_7	Address Inputs
O_0–O_3	Data Outputs

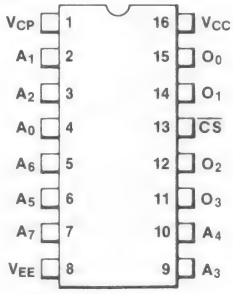
Logic Symbol



V_{CP} = Pin 1
V_{CC} = Pin 16
V_{EE} = Pin 8

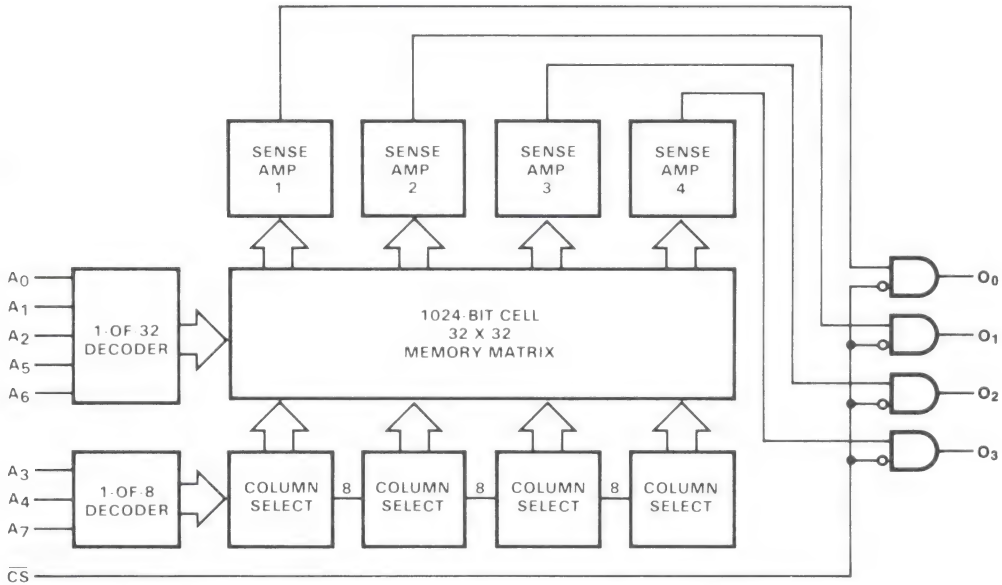
Connection Diagram

16-Pin DIP (Top View)



Note
The Flatpak version has the same pinout (Connection Diagram) as the Dual In-line Package.

Logic Diagram



Functional Description

The F10Z416 is a fully decoded bipolar field programmable read only memory organized 256 words by four bits per word. An unterminated emitter-follower output is provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many F10Z416 devices can be tied together. An external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is off.

One Chip Select ($\overline{CS}$) input is provided for memory array expansion up to 512 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of $\overline{CS}$ from the address without increasing address access time. The device is enabled when $\overline{CS}$ is LOW. When the device is disabled ($\overline{CS}$ = HIGH), all outputs are forced LOW.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the A_0 through A_7 inputs, the chip is selected and data is valid at the outputs after t_{AA}.

The F10Z416 uses open base transistor vertical (junction) fuse cells. Initially, an unprogrammed cell is in the logic '1' state. Cells can selectively be programmed to a logic '0' state by following a specified procedure which fuses aluminum through the emitter-base junction of the cell transistor.

Note: Consult factory for ordering information

Notes

Absolute Maximum Ratings: Above which the useful life may be impaired

Storage Temperature	−65° to +150° C
Supply Voltage Range	−0.5 V to +7.0 V
Input Voltage (dc)[1][2]	−0.5 V to V_{CC} (RAMs)
	−1.5 V to V_{CC} (PROMs)
Voltage Applied to Outputs[2][3] (output HIGH)	−0.5 V to +5.5 V (RAMs)
	−1.5 V to +5.5 V (PROMs)
Lead Temperature (Soldering, 10 sec)	300° C
Maximum Junction Temperature (T_j)	+175° C
Output Current	+20mA
Input Current (DC)	-12 mA to +5.0 mA

Guaranteed Operating Ranges

	Supply Voltage (V_{CC})	Case Temperature (T_C)	Maximum Low-Level Input Voltage (V_{IL})[8]	Minimum High-Level Input Voltage (V_{IH})[8]
Commercial	5.0 V ± 5%	0° C to +75° C	0.8V	2.1 V (RAMs) 2.0V (PROMs)
Military	5.0 V ± 10%	-55° C to +125° C		

Device Design Characteristics

Symbol	Characteristic	Typ	Unit	Condition
C_{IN}	Input Pin Capacitance	4.0	pF	Measured with a Pulse
C_{OUT}	Output Pin Capacitance	7.0	pF	Technique

DC, FN and AC performance characterisics and test conditions listed with each device. (See note 8)

Notes
1. Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
2. These values may be exceeded as required during PROM programming.
3. Output current limit required.
4. Unless stated otherwise in individual device specification.
5. Funtional testing done at input levels $V_{IL} = V_{OL\ MAX}$ (0.45 V), $V_{IH} = V_{OH\ MIN}$ (2.4 V).
6. PROM programmability verified through test row and test column.
7. PROM input levels on unprogrammed devices verified through testing of test row and test column.
8. Static condition only.

FAIRCHILD
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93Z450/93Z451
1024 x 8-Bit Programmable Read Only Memory

Memory and High Speed Logic

Description

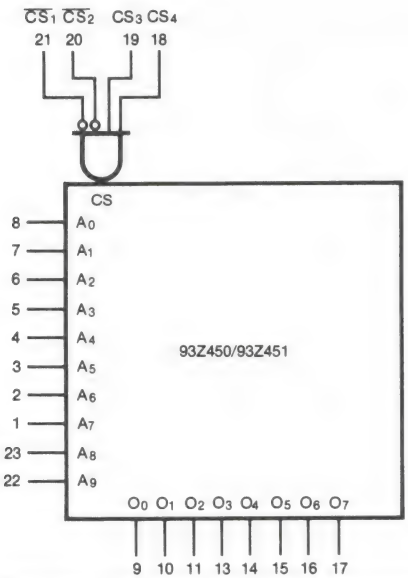
The 93Z450 and 93Z451 are fully decoded 8,192-bit Programmable Read Only Memories (PROMs), organized 1024 words by eight bits per word. The two devices are identical except the 93Z450 has open collector outputs while the 93Z451 has three state outputs. Both devices are available in two speed versions, standard speed and 'A' grade.

- **Commercial Address Access Time**
  93Z450/93Z451 — 40 ns Max
  93Z450A/93Z451A — 35 ns Max
- **Military Address Access Time**
  93Z450/93Z451 — 55 ns Max
  93Z450A/93Z451A — 45 ns Max
- **Highly Reliable Vertical Fuses Ensure High Programming Yields**
- **Available with Open Collector (93Z450) or Three State (93Z451) Outputs**
- **Low Current PNP Inputs**

Pin Names

A_0–A_9	Address Inputs
$\overline{CS}_1$, $\overline{CS}_2$	Chip Select Inputs (Active LOW)
CS_3, CS_4	Chip Select Inputs (Active HIGH)
O_0–O_7	Data Outputs

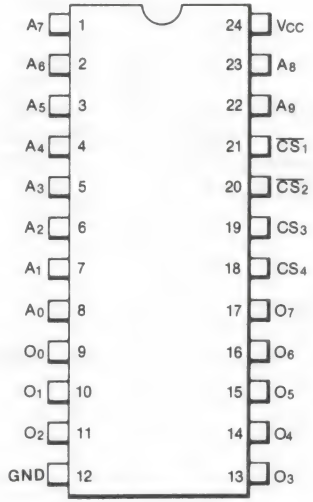
Logic Symbol



VCC = Pin 24
GND = Pin 12

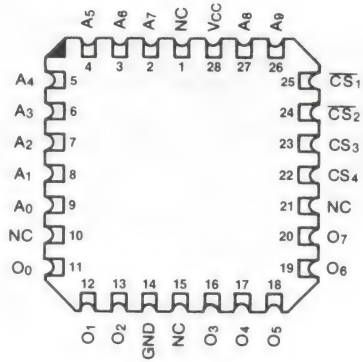
Connection Diagrams

24-pin DIP (Top View)

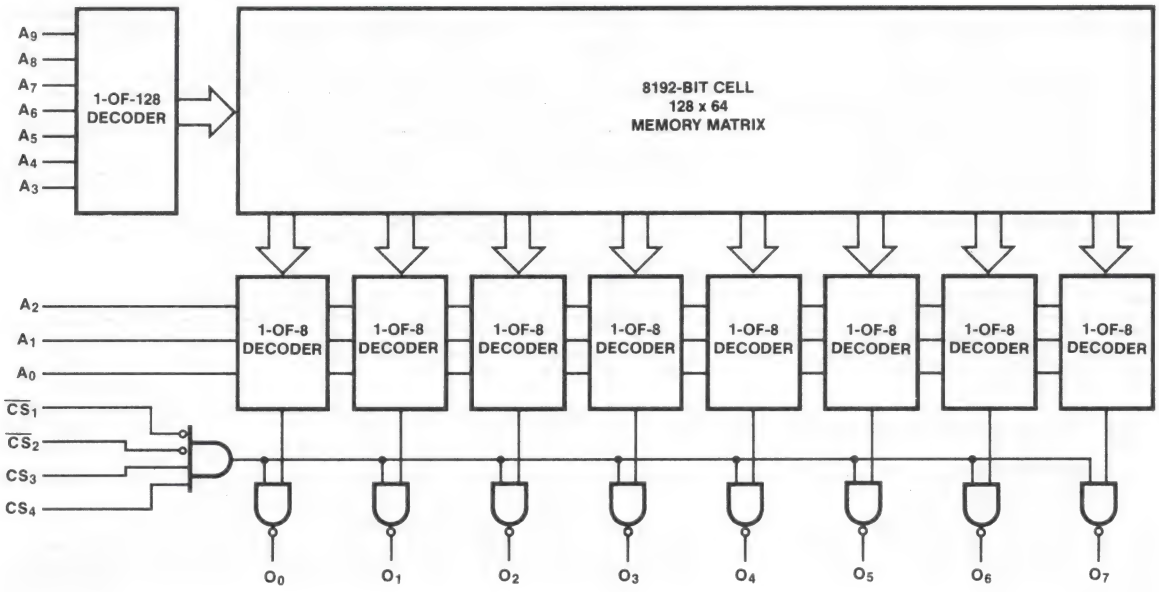


Note:
The 24-pin Flatpak has the same pinout (Connection Diagram) as the 24-pin DIP.

28-pin Leadless Chip Carrier (Top View)



Logic Diagram



Functional Description

The 93Z450 and 93Z451 are TTL bipolar field Programmable Read Only Memories (PROMs) organized 1024 words by eight bits per word. Open-collector outputs are provided on the 93Z450 for use in wired-OR applications. The 93Z451 has 3-state outputs which provide active pull ups when enabled and high output impedance when disabled. This allows optimization of word expansion in bus organized systems.

Four Chip Select inputs are provided for logic flexibility and for memory array expansion of up to 128K without the need for external decoding. The fast Chip Select access time permits direct address decoding without increasing overall memory access times. Both devices are enabled only when $\overline{CS}_1$ and $\overline{CS}_2$ are LOW and CS_3 and CS_4 are HIGH.

The devices contain an internal test row and test column which are accessed and programmed during both wafer sort and final test. These test fuses are used to assure high programmability and to guarantee AC performance and DC parameters.

The 93Z450 and 93Z451 use open base vertical transistor (junction) fuse cells. Initially an unprogrammed cell is in the logic '0' state. Cells can be programmed to a logic '1' state by following the specified programming procedure which fuses aluminum through the emitter base junction of the cell transistor.

The read function is identical to that of a conventional Read Only Memory (ROM). A binary address is applied to the address pins A_0 through A_9 and the chip is selected. Data is then available at the outputs after t_{AA}.

DC Performance Characteristics: Over guaranteed operating ranges unless otherwise noted

Symbol	Characteristic	Min	Typ(1)	Max	Unit	Condition
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IC}	Input Clamp Diode Voltage			−1.2	V	V_{CC} = Min, I_{IN} = −18 mA
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = Min, I_{OL} = 16 mA
V_{OH}	Output HIGH Voltage (93Z451)	2.4			V	V_{CC} = Min, I_{OH} = −2.0 mA Address Any '1'
I_{IL}	Input LOW Current		−10	−100	μA	V_{CC} = Max, V_{IL} = 0.45 V
I_{IH}	Input HIGH Current	−40		40	μA	V_{CC} = Max, V_{IH} = 2.4 V to V_{CC}
I_{OHZ} I_{OLZ}	Output Leakage Current for High Impedance State (93Z451)			40 −40	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V
I_{CEX}	Output Leakage Current (93Z450)			40	μA	V_{CEX} = V_{CC}, Chip Deselected
I_{OS}	Output Short-Circuit Current (93Z451)	−20	−45	−90	mA	V_{CC} = Max, V_O = 0 V, Note 2 Address Any '1'
I_{CC}	Power Supply Current		110	135	mA	V_{CC} = Max, Inputs Grounded, Outputs Open

Commercial

AC Performance Characteristics: V_{CC} = 5.0 V ± 5%, GND = 0 V, T_C = 0°C to +75°C

Symbol	Characteristic	'A'	Std	Unit	Condition
t_{AA}	Address to Output Access Time	35	40	ns	See AC Output Load
t_{ACS}	Chip Select to Output Access Time	25	30	ns	See AC Output Load

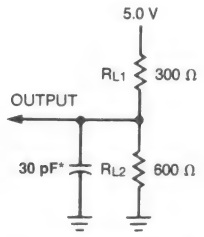
Military

AC Performance Characteristics: V_{CC} = 5.0 V ± 10%, GND = 0 V, T_C = −55°C to +125°C

Symbol	Characteristic	'A'	Std	Unit	Condition
t_{AA}	Address to Output Access Time	45	55	ns	See AC Output Load
t_{ACS}	Chip Select to Output Access Time	30	35	ns	See AC Output Load

1. Typical values are at V_{CC} = 5.0 V, T_C = +25° C.
2. Not more than one output to be shorted at a time. Duration of the short circuit should not exceed one second.

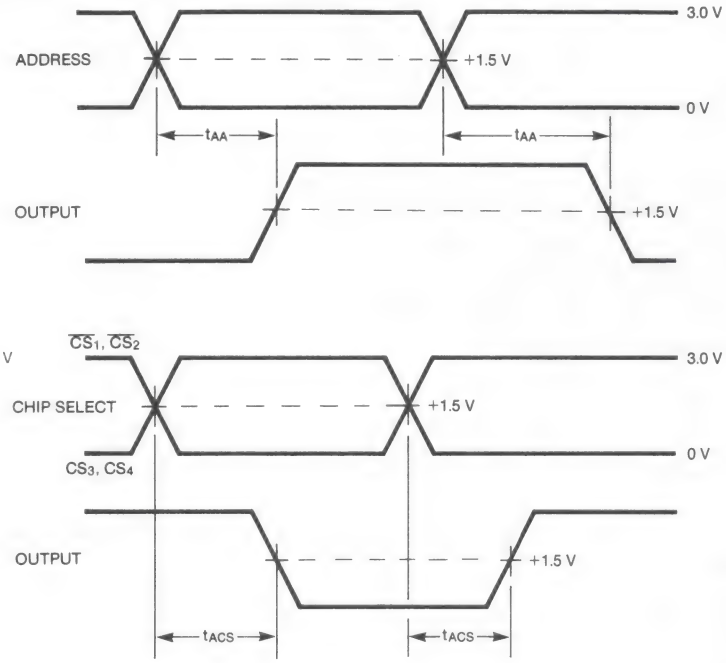
Fig. 1 AC Test Output Load



*Includes jig and probe capacitance

Test Conditions
Input pulse: 0 V to 3.0 V
Input pulse rise and fall times: 5 ns between 1 V and 2 V
Measurements made at 1.5 V level

Fig. 2 AC Waveforms



Ordering Information

93Z450
93Z451 A SD M

Device Name
Speed Selection
Package
Temperature Range
Optional Processing

Speed Selection
Blank = Standard Speed
A = 'A' Grade

Packages and Outlines (See Section 9)
D = 24-pin Ceramic DIP
P = 24-pin Plastic DIP (Commercial only)
SD = 24-pin Slim Ceramic DIP
F = 24-pin Flatpak
L = 28-pin Square Leadless Chip Carrier

Temperature Range
C = 0°C to +75°C
M = −55°C to +125°C

Optional Processing
QB = Mil Std 883B
Method 5004 and 5005, Level B
QR = Commercial Device with
160 Hour Burn In or Equivalent

7

FAIRCHILD
A Schlumberger Company

93Z510/93Z511
2048 x 8-Bit Programmable Read Only Memory

Memory and High Speed Logic

Description

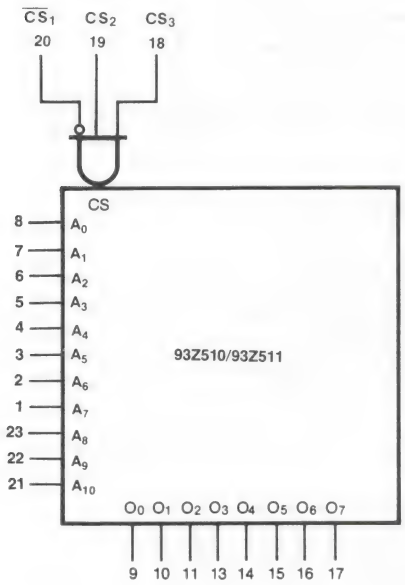
The 93Z510 and 93Z511 are fully decoded 16,384-bit Programmable Read Only Memories (PROMs), organized 2048 words by eight bits per word. The two devices are identical except the 93Z510 has open collector outputs while the 93Z511 has three state outputs.

- **Commercial Address Access Time — 45 ns Max**
- **Military Address Access Time — 55 ns Max**
- **Highly Reliable Vertical Fuses Ensure High Programming Yields**
- **Available with Open Collector (93Z510) or Three State (93Z511) Outputs**
- **Low Current PNP Inputs**

Pin Names

A_0–A_{10}	Address Inputs
$\overline{CS}_1$	Chip Select Input (Active LOW)
CS_2, CS_3	Chip Select Inputs (Active HIGH)
O_0–O_7	Data Outputs

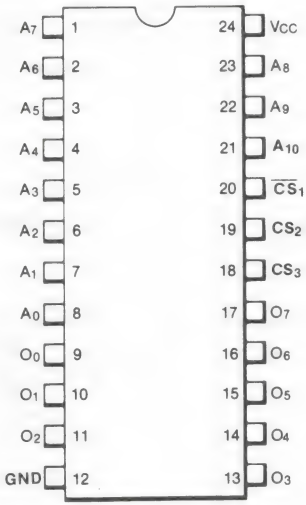
Logic Symbol



Vcc = Pin 24
GND = Pin 12

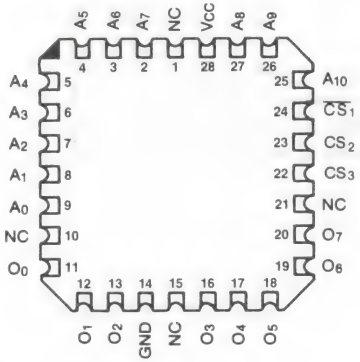
Connection Diagrams

24-pin DIP (Top View)

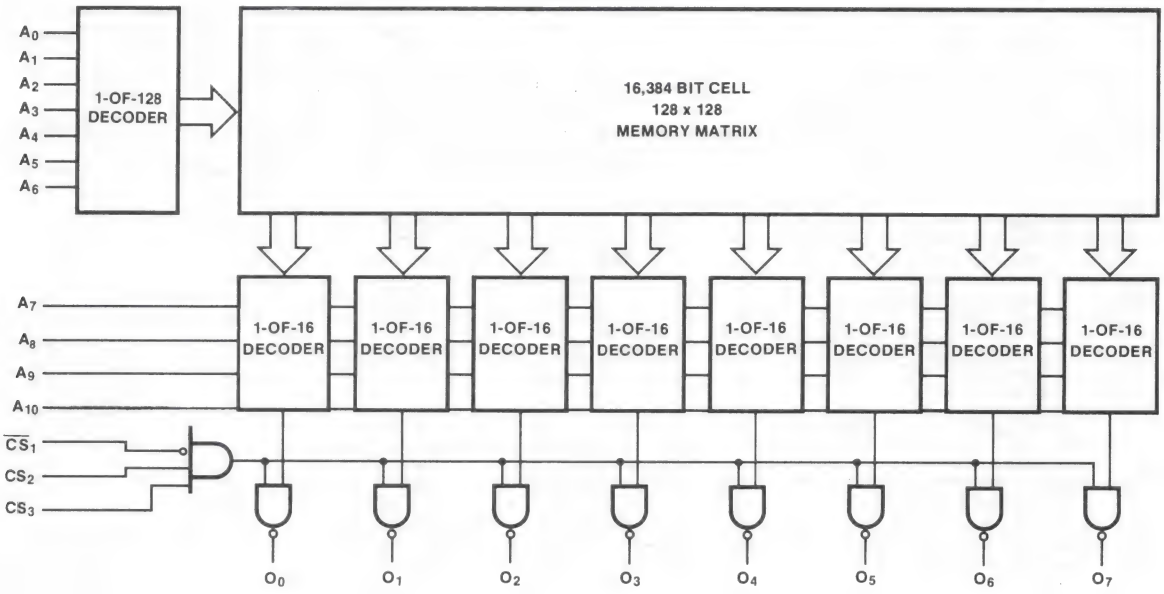


Note:
The 24-pin Flatpak has the same pinout (Connection Diagram) as the 24-pin DIP.

28-pin Leadless Chip Carrier (Top View)



Logic Diagram



Functional Description

The 93Z510 and 93Z511 are TTL bipolar field Programmable Read Only Memories (PROMs) organized 2048 words by eight bits per word. Open-collector outputs are provided on the 93Z510 for use in wired-OR applications. The 93Z511 has 3-state outputs which provide active pull ups when enabled and high output impedance when disabled. This allows optimization of word expansion in bus organized systems.

Three Chip Select inputs are provided for logic flexibility and for memory array expansion of up to 128K without the need for external decoding. The fast Chip Select access time permits direct address decoding without increasing overall memory access times. Both devices are enabled only when $\overline{CS}_1$ is LOW and CS_2 and CS_3 are HIGH.

The devices contain an internal test row and test column which are accessed and programmed during both wafer sort and final test. These test fuses are used to assure high programmability and to guarantee AC performance and DC parameters.

The 93Z510 and 93Z511 use open base vertical transistor (junction) fuse cells. Initially an unprogrammed cell is in the logic '0' state. Cells can be programmed to a logic '1' state by following the specified programming procedure which fuses aluminum through the emitter base junction of the cell transistor.

The read function is identical to that of a conventional Read Only Memory (ROM). A binary address is applied to the address pins A_0 through A_{10} and the chip is selected. Data is then available at the outputs after t_{AA}.

DC Performance Characteristics: Over guaranteed operating ranges unless otherwise noted

Symbol	Characteristic	Min	Typ(1)	Max	Unit	Condition
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IC}	Input Clamp Diode Voltage			−1.2	V	V_{CC} = Min, I_{IN} = −18 mA
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = Min, I_{OL} = 16 mA
V_{OH}	Output HIGH Voltage (93Z511 only)	2.4			V	V_{CC} = Min, I_{OH} = −2.0 mA Address Any '1'
I_{IL}	Input LOW Current		−10	−100	μA	V_{CC} = Max, V_{IL} = 0.45 V
I_{IH}	Input HIGH Current	−40		40	μA	V_{CC} = Max, V_{IH} = 2.4 V to V_{CC}
I_{OHZ} I_{OLZ}	Output Leakage Current for High Impedance State (93Z511 only)			40 −40	μA	V_{OH} = 2.4 V V_{OL} = 0.4 V
I_{CEX}	Output Leakage Current (93Z510 only)			40	μA	V_{CEX} = V_{CC} Chip Deselected
I_{OS}	Output Short-Circuit Current (93Z511 only)	−15	−35	−90	mA	V_{CC} = Max, V_O = 0 V, Note 2 Address Any '1'
I_{CC}	Power Supply Current		120	175	mA	V_{CC} = Max All Inputs GND All Outputs Open

Commercial

AC Performance Characteristics: V_{CC} = 5.0 V ± 5%, GND = 0 V, T_C = 0°C to +75°C

Symbol	Characteristic	Max	Unit	Condition
t_{AA}	Address to Output Access Time	45	ns	See AC Output Load
t_{ACS}	Chip Select to Output Access Time	25	ns	See AC Output Load

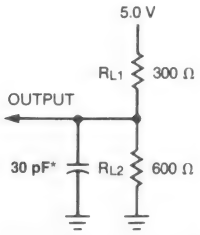
Military

AC Performance Characteristics: V_{CC} = 5.0 V ± 10%, GND = 0 V, T_C = −55°C to +125°C

Symbol	Characteristic	Max	Unit	Condition
t_{AA}	Address to Output Access Time	55	ns	See AC Test Output Load
t_{ACS}	Chip Select to Output Access Time	25	ns	See AC Test Output Load

1. Typical values are at V_{CC} = 5.0 V, T_C = +25°C.
2. Not more than one output to be shorted at a time. Duration of the short circuit should not exceed one second.

Fig. 1 AC Test Output Load

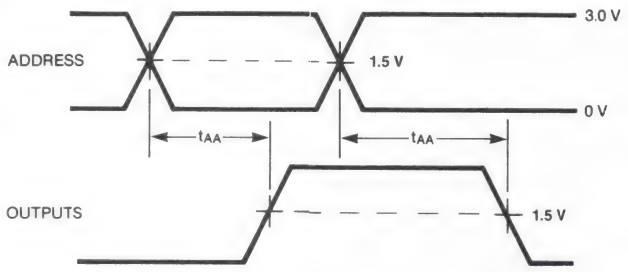


*Includes jig and probe capacitance

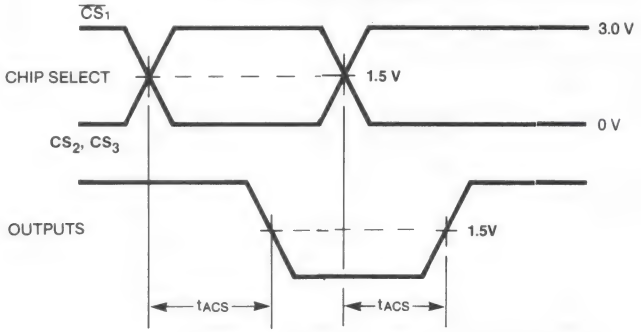
Test Conditions
Input pulse: 0 V to 3.0 V
Input pulse rise and fall times: 5 ns between 1 V and 2 V
Measurements made at 1.5 V level

Fig. 2 AC Waveforms

2a Propagation Delay from Address Inputs



2b Propagation Delay from Chip Select



Ordering Information

93Z510
93Z511 D M

Device Name
Package
Temperature Range
Optional Processing

Packages and Outlines (See Section 9)
D = Ceramic DIP
F = Flatpak
L = Leadless Chip Carrier
P = Plastic DIP
SD = Slim Ceramic DIP

Temperature Ranges
C = 0°C to +75°C
M = −55°C to +125°C

Optional Processing
QB = Mil Std 883
Method 5004 & 5005, Level B

QR = Commercial Device with
160 Hour Burn In or Equivalent

FAIRCHILD
A Schlumberger Company

93Z564/93Z565
8192 x 8-Bit Programmable Read Only Memory

Memory and High Speed Logic

Description

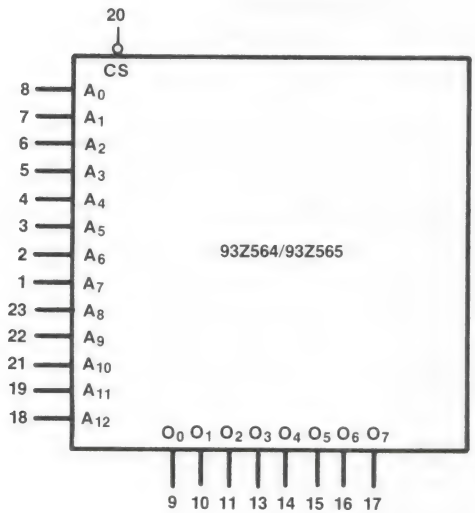
The 93Z564 and 93Z565 are fully decoded 65,536-bit Programmable Read Only Memories (PROMs), organized 8192 words by eight bits per word. The two devices are identical except the 93Z564 has open collector outputs while the 93Z565 has three state outputs. Both devices are available in two speed versions, standard speed and 'A' grade.

- **Commercial Address Access Time**
  93Z564/93Z565 — 55 ns Max
  93Z564A/93Z565A — 45 ns Max
- **Military Address Access Time**
  93Z564/93Z565 — 65 ns Max
  93Z564A/93Z565A — 55 ns Max
- **Highly Reliable Vertical Fuses Ensure High Programming Yields**
- **Available with Open Collector (93Z564) or Three State (93Z565) Outputs**
- **Low Current PNP Inputs**

Pin Names

A_0–A_{12}	Address Inputs
$\overline{CS}$	Chip Select Input (Active LOW)
O_0–O_7	Data Outputs

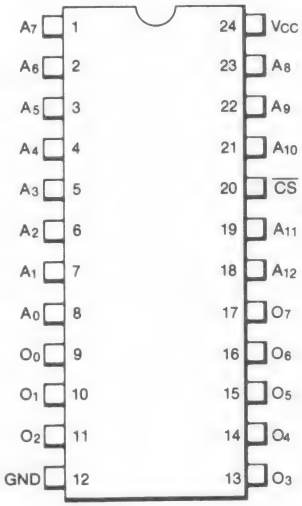
Logic Symbol



V_{CC} = Pin 24
GND = Pin 12

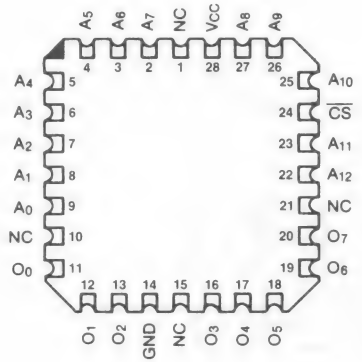
Connection Diagrams

24-pin DIP (Top View)

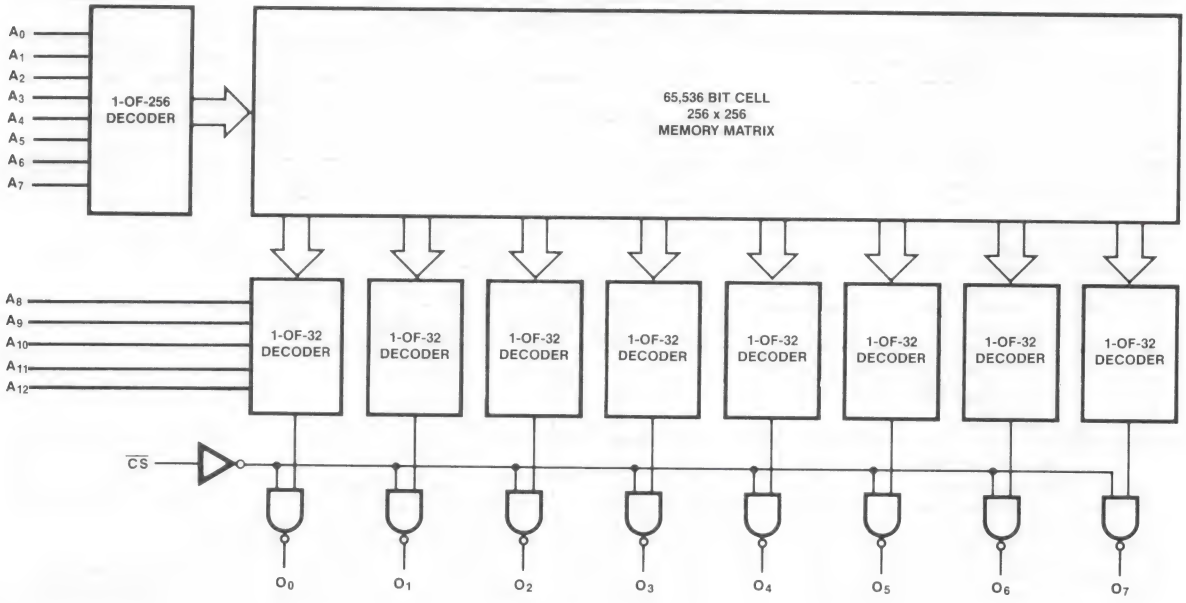


Note:
The 24-pin Flatpak has the same pinout (Connection Diagram) as the 24 pin DIP.

28-pin Leadless Chip Carrier (Top View)



Logic Diagram



Functional Description

The 93Z564 and 93Z565 are TTL bipolar field Programmable Read Only Memories (PROMs) organized 8192 words by eight bits per word. Open-collector outputs are provided on the 93Z564 for use in wired-OR applications. The 93Z565 has 3-state outputs which provide active pull ups when enabled and high output impedance when disabled. This allows optimization of word expansion in bus organized systems.

One Chip Select input is provided for logic flexibility and for memory array expansion of up to 128K without the need for external decoding. The fast Chip Select access time permits direct address decoding without increasing overall memory access times. Both devices are enabled only when $\overline{CS}$ is LOW.

The devices contain an internal test row and test column which are accessed and programmed during both wafer sort and final test. These test fuses are used to assure high programmability and to guarantee AC performance and DC parameters.

The 93Z564 and 93Z565 use open base vertical transistor (junction) fuse cells. Initially an unprogrammed cell is in the logic '0' state. Cells can be programmed to a logic '1' state by following the specified programming procedure which fuses aluminum through the emitter base junction of the cell transistor.

The read function is identical to that of a conventional Read Only Memory (ROM). A binary address is applied to the address pins A_0 through A_{12} and the chip is selected. Data is then available at the outputs after t_{AA}.

DC Performance Characteristics: Over guaranteed operating ranges unless otherwise noted

Symbol	Characteristic	Min	Typ(1)	Max	Unit	Condition
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IC}	Input Clamp Diode Voltage			−1.2	V	V_{CC} = Min, I_{IN} = −18 mA
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = Min, I_{OL} = 16 mA
V_{OH}	Output HIGH Voltage (93Z565 only)	2.4			V	V_{CC} = Min, I_{OH} = −2.0 mA Address Any '1'
I_{IL}	Input LOW Current		−10	−100	μA	V_{CC} = Max, V_{IL} = 0.45 V
I_{IH}	Input HIGH Current	−40		40	μA	V_{CC} = Max, V_{IH} = 2.4 V to V_{CC}
I_{OHZ} I_{OLZ}	Output Leakage Current for High Impedance State (93Z565 only)			40 −40	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V
I_{CEX}	Output Leakage Current (93Z564 only)			40	μA	V_{CEX} = V_{CC} Chip Deselected
I_{OS}	Output Short-Circuit Current (93Z565 only)	−15	−35	−90	mA	V_{CC} = Max, V_O = 0 V, Note 2 Address Any '1'
I_{CC}	Power Supply Current		120	180	mA	V_{CC} = Max, All Inputs GND, All Outputs Open
C_{IN}	Input Pin Capacitance		7.0(3)		pF	V_{CC} = 5.0 V, V_{IN} = 4.0 V, f = 1.0 MHz
C_O	Output Pin Capacitance		10.0(3)		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz

Commercial
AC Performance Characteristics: V_{CC} = 5.0 V ± 5%, GND = 0 V, T_C = 0° C to +75° C

Symbol	Characteristic	'A'	Std	Unit	Condition
t_{AA}	Address to Output Access Time	45	55	ns	See AC Output Load
t_{ACS}	Chip Select to Output Access Time	25	30	ns	See AC Output Load

Military
AC Characteristics: V_{CC} = 5.0 V ± 10%, GND = OV, T_C = -55°C to + 125°C

Symbol	Characteristic	'A'	Std	Unit	Condition
t_{AA}	Address to Output Access Time	55	65	ns	See AC Output Load
t_{ACS}	Chip Select to Output Access Time	30	35	ns	See AC Output Load

1. Typical values are at V_{CC} = 5.0 V, T_C = +25° C.
2. Not more than one output to be shorted at a time. Duration of the short circuit should not exceed one second.
3. This parameter value is based on initial design qualification and is also verified on every design change. These are not tested in production.

Fig. 1 AC Waveforms

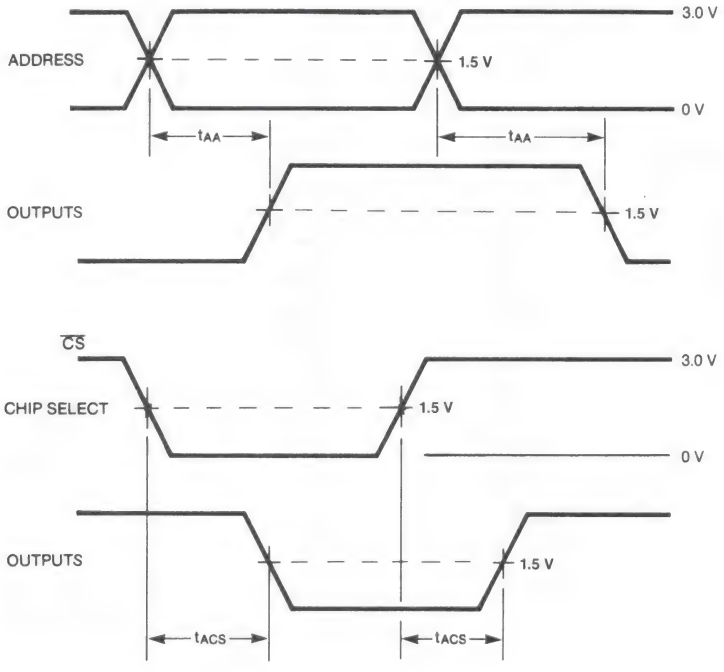
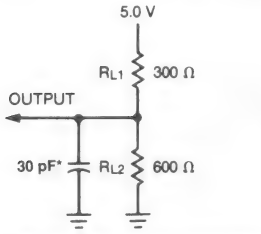


Fig. 2 AC Test Output Load



*Includes jig and probe capacitance

Test Conditions
Input Pulse: 0 V to 3.0 V
Input Pulse Rise and Fall Times: 5 ns between 1 V and 2 V
Measurements made at 1.5 V Level

Ordering Information

93Z564
93Z565 A D M

Device Name
Speed Selection
Package
Temperature Range
Optional Processing

Speed Selection
Blank = Standard Speed
A = 'A' Grade

Packages
D = Ceramic DIP
L = Leadless Chip Carrier

Temperature Ranges
C = 0°C to +75°C
M = −55°C to +125°C

Optional Processing
QB = Mil Std 883
Method 5004 & 5005, Level B
QR = Commercial Device with
160 Hour Burn In or Equivalent

7

FAIRCHILD
A Schlumberger Company

93Z611
2048 x 8-Bit Programmable Read Only Memory

Memory and High Speed Logic

Description

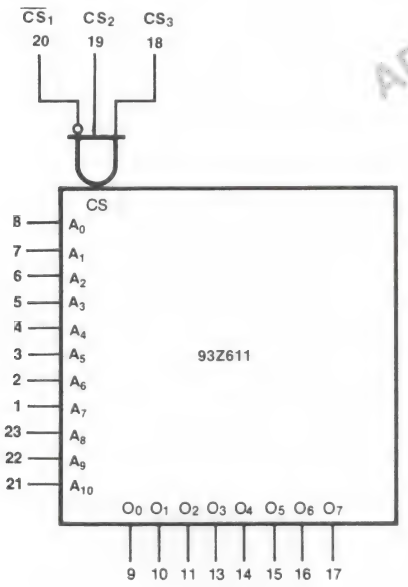
The 93Z611 is a fully decoded 16,384-bit Programmable Read Only Memory (PROM), organized 2048 words by eight bits per word. The 93Z611 is manufactured using Fairchild's highly reliable FAST-Z vertical fuse technology.

- **Available in 300 and 600 mil Cerdip, Plastic DIP, LCC and flatpak**
- **Commercial Address Access Time — 25 ns Max**
- **Military Address Access Time — 30 ns Max**
- **Highly Reliable Vertical Fuses Ensure High Programming Yields**
- **Low Current PNP Inputs**
- **Power-Up Three-State Outputs**

Pin Names

A_0–A_{10}	Address Inputs
$\overline{CS}_1$	Chip Select Input (Active LOW)
CS_2, CS_3	Chip Select Inputs (Active HIGH)
O_0–O_7	Data Outputs

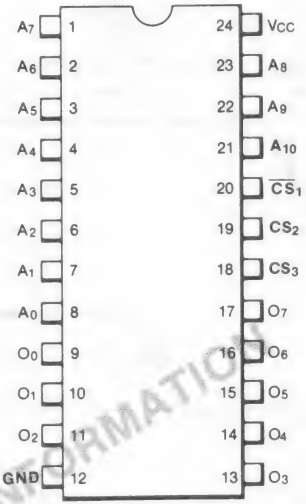
Logic Symbol



V_{CC} = Pin 24
GND = Pin 12

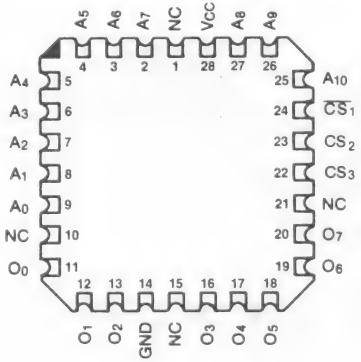
Connection Diagrams

24-pin DIP (Top View)



Note:
The 24-pin Flatpak has the same pinout (Connection Diagram) as the 24-pin DIP.

28-pin Leadless Chip Carrier (Top View)



FAIRCHILD
A Schlumberger Company

93Z667
8192 x 8-Bit Programmable Read Only Memory

Memory and High Speed Logic

Description

The 93Z667 is a fully decoded 65,384-bit Programmable Read Only Memories (PROMs), organized 8192 words by eight bits per word. The 93Z667 is manufactured using Fairchild's highly reliable FAST-Z vertical fuse technology.

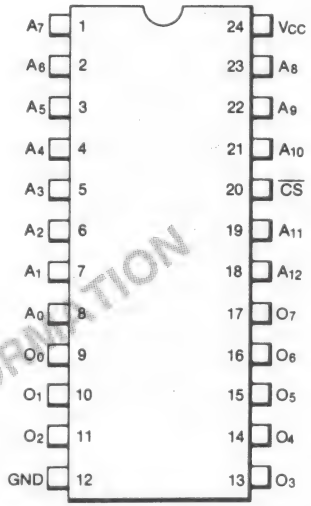
- **Available in 300 mil Side-Brazed DIP,**
- **Commercial Address Access Time — 40 ns Max**
- **Military Address Access Time — 45 ns Max**
- **Highly Reliable Vertical Fuses Ensure High Programming Yields**
- **Power-Up Three State Outputs**
- **Low Current PNP Inputs**

Pin Names

A_0–A_{12}	Address Inputs
$\overline{CS}$	Chip Select Input (Active LOW)
O_0–O_7	Data Outputs

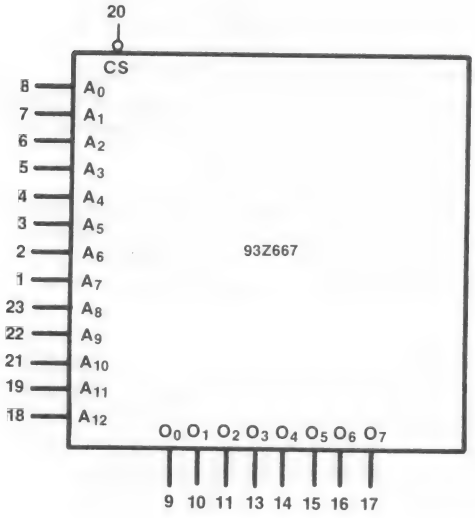
Connection Diagrams

24-pin DIP (Top View)



Note:
The 24-pin Flatpak has the same pinout (Connection Diagram) as the 24 pin DIP.

Logic Symbol



VCC = Pin 24
GND = Pin 12

7

Isoplanar-Z Junction Fuse Principles and Programming

Conventional fusible link bipolar PROMs and programmable logic devices are based upon two dimensional matrices of electrically conductive thin film fusible elements of materials such as nichrome, titanium tungsten, platinum silicide or polysilicon. Each of these thin film technologies has its own unique advantages and disadvantages but all have in common the fact that fuses lie flat on the surface of the silicon and therefore occupy a significant portion of silicon area. Cell area has become increasingly important as device densities have grown from 4K to 64K. Manufacturing cost, yields and performance are all directly related to die size which is a strong function of cell area. Previously, reductions in cell area have been accomplished primarily through improvements in photolithographic techniques. Such techniques have been pushed to their limits to produce high density, cost effective programmable memories and logic. The need to shrink cell sizes, especially in higher density devices, is placing severe strains on the manufacturability of thin film fuses.

Junction fuses are the emerging solution to the inherent problems posed by thin film fuses. A junction fuse is simply a PN junction programmable cell. The emitter-base junction of a floating base NPN transistor acts as the fuse element. Because fuses are single vertical transistors (hence the often used name of vertical fuses), they occupy minimal silicon area. The entire fuse structure can essentially be modeled as two diodes connected back-to-back. Before programming, a high impedence (open) path exists between the emitter and collector. The emitter-base diode is reverse biased, preventing read currents from passing through the fuse. During programming, the emitter-base junction is shorted out, leaving a forward biased base-collector (B-C) diode. This diode now appears as a low impedence (closed) path. The fuse junction lies beneath the surface of the silicon so all of the potential thin film fuse related failure modes such as metal migration (growback), freeze out, corrosion, marginally opened fuses and passivation scattering have been eliminated.

The major problem encountered in early P-N junction programmable junction fuse development was the requirement of a large cell programming current (typically 200 mA per cell). This large current meant that large transistors were needed in the peripheral programming circuitry. The gain in array size reduction due to small cells was offset by the need for a larger peripheral programming circuitry which, in turn, translated to larger overall die size and higher die cost. The costs were such that, despite their reliability advantages, these devices were never widely commercially accepted.

The most straightforward method to achieve reductions in cell programming current is to use small emitter cells. A small emitter cell increases the effective current density at the emitter-base junction therefore decreasing the overall energy required to program the cell. To reduce emitter size and programming currents without the use of advanced photolithographic equipment, Fairchild adopted a simple solution, use a walled emitter cell and an oxide isolated Isoplanar process. With oxide isolation, emitter sizes are defined by the oxide opening and as a result are self aligned, easing manufacturing tolerances.

The main advantages of the Isoplanar-Z process are due to the use of oxide encroachment. The cell emitter is defined using standard photolithography. The surrounding oxide is then laterally grown, shrinking the emitter area and decreasing the effective cell size. Very small self aligned emitter-base junction areas can be achieved quite easily with the encroachment technique. An added benefit of oxide encroachment is that the higher thermal resistivity of the silicon dioxide which surrounds the cells, as compared to silicon, reduces heat loss during programming. This thermal insulation effect further reduces the current required to program a cell. Typical programming currents of 60 mA or below are easily achieved using the Isoplanar-Z process.

Results of reliability and programming yield testing have been excellent. Data have demonstrated typical programming yields in excess of 99% on a 16,384 bit PROM and no cell related failures in over 63 billion cell hours of life test.

Programming a Junction Fuse

Programming a junction fuse is accomplished by driving a controlled current through the emitter of the cell, inducing avalanche breakdown of the emitter-base junction. Heat locally generated at the reverse biased junction causes the Aluminum-Silicon interface to reach the

Al-Si eutectic solidus (melting) temperature of approximately 575°C. The electrically conductive aluminum eutectic then diffuses down through the emitter to the emitter-base junction, forming a permanent short.

The amount of energy required to program a cell is dependent upon encroachment variations. Different methods can be used to supply the varying amount of energy required to program junction fuses. One method is a pulse-read technique, whereby a series of energy pulses of increasing magnitude or duration are applied to the cell. Each pulse applies a specific amount of energy to the cell's emitter-base junction, successively heating the junction until the cell emitter reaches the Aluminum-Silicon eutectic temperature. Once this temperature is reached, migration occurs and the junction shorts. A read is performed after each pulse to detect if the fuse has blown. If additional energy is needed to program any cell, more pulses are applied until the cell blows.

Fairchild has approved a current-pulse technique for users with digital requirements. In this method, differences in required programming energy are accounted for by increasing the current amplitude of each subsequent current pulse until programming is achieved. A read is performed after each pulse. This cycle is continued until the cell is programmed. Refer to the Programming Timing Diagram and Programming Specifications for Current-Pulse Programming.

Fairchild originally developed a self adjusting current ramp programming technique which delivers the optimum current needed to program each individual cell. With the self adjusting technique a steadily increasing current ramp is applied to a cell until a shorted junction is detected. The exact moment when the junction actually shorts can be sensed by a sharp drop in the voltage across the cell. This voltage drop occurs because the reverse biases E-B diode is no longer in series with the programming path.

Once the moment of programming has been detected, Fairchild incorporates the use of a programming ramp "post hold time". The rise in programming current is halted at the level which was required to cause a blow, held for a precise time interval, and then turned off. This means that the amount of additional energy applied to a cell is totally governed by the amount of current required to program that cell, which is in turn dependent upon cell size. Therefore each cell's additional energy pulse is custom tailored for that specific cell. Experimental data shows that a carefully chosen post hold time can insure a very uniform cell resistance regardless of cell size. The self adjusting current ramp programming scheme allows consistent, repeatable programming and uniform cell resistance, overcoming any effects of process variations on a particular product or differences in cell sizes across product lines. Refer to the Programming Timing Diagram and Programming Specifications for Current-Ramp Programming.

FAIRCHILD
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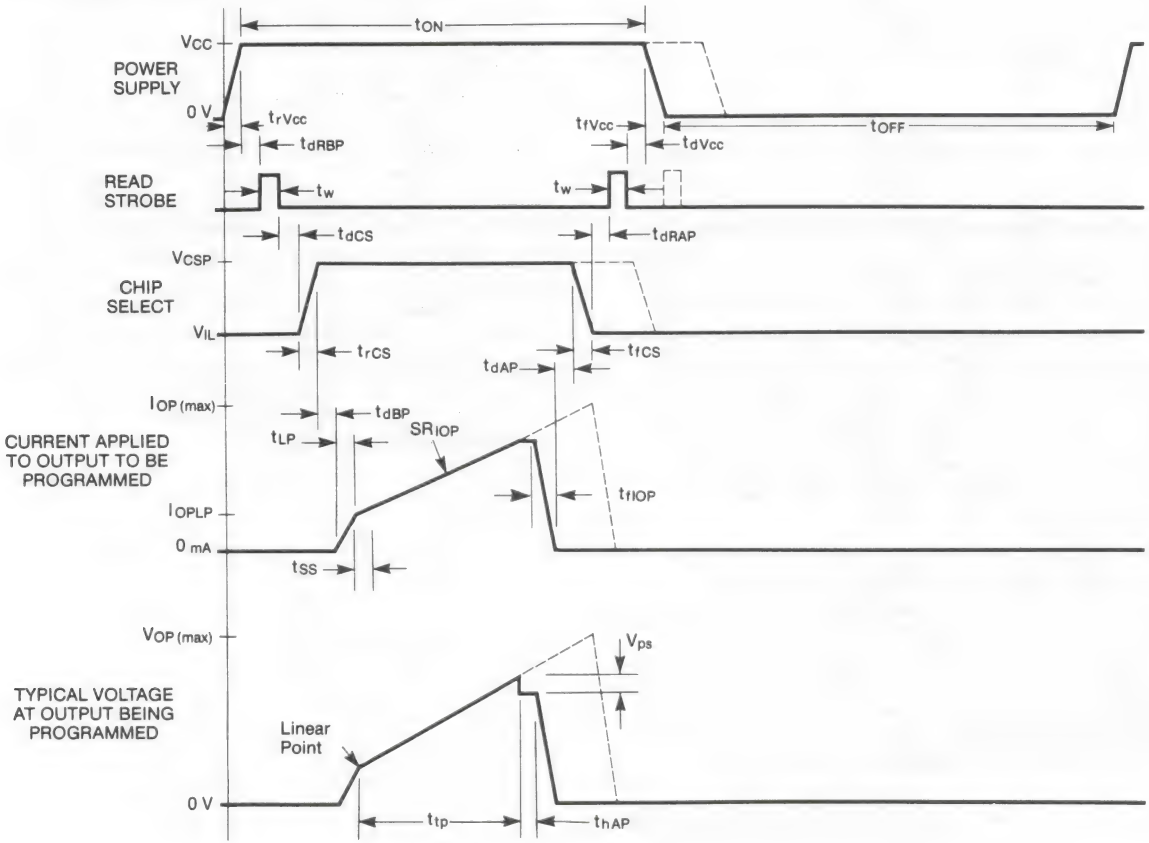
Isoplanar-Z TTL PROM Current-Ramp Programming Specifications

Current-Ramp Programming Timing Diagram



Current-Ramp Programming Specifications[4]

Symbol	Parameter	Min	Recommended Value	Max	Units	Comments
Power Supply						
V_{CC}	Power Supply Voltage	6.4	6.5	6.6	V	Typical I_{CC} at 6.5 V = 250 mA
t_{rVcc}	Power Supply Rise Time[3]	0.2	2.0		μs	
t_{fVcc}	Power Supply Fall Time	0.2	2.0		μs	
t_{ON}	V_{CC} On Time	(1)				See Programming Timing Diagram
t_{OFF}	V_{CC} Off Time	(2)				
	Duty Cycle for V_{CC}			50	%	$t_{ON}/(t_{OFF} + t_{ON})$

Current-Ramp Programming Specifications[4] (Cont'd)

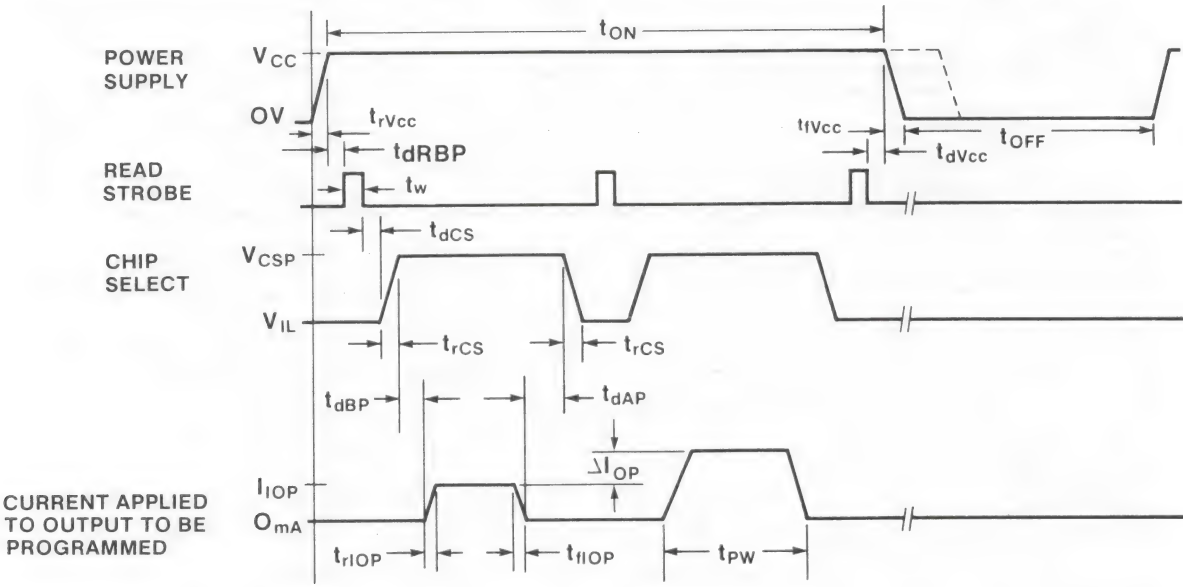
Symbol	Parameter	Min	Recommended Value	Max	Units	Comments
Read Strobe						
t_{dRBP}	Read Delay before Programming		3.0		μs	Initial Check
t_w	Fuse Read Time		1.0		μs	
t_{dVcc}	Delay to V_{CC} Off		1.0		μs	
t_{dRAP}	Delay to Read after Programming		3.0		μs	Verify
Chip Select						
V_{CSP}	Chip Select Programming Voltage	20.0	20.0	22.0	V	
I_{CSP}	Chip Select Program Current Limit	175	180	185	mA	
V_{IL}	Input Voltage LOW	0	0	0.4	V	
V_{IH}	Input Voltage HIGH	2.4	5.0	5.0	V	
t_{dCS}	Delay to Chip Deselect		1.0		μs	
t_{rCS}	Chip Select Pulse Rise Time	3.0	4.0		μs	
t_{dAP}	Delay to Chip Select Time	0.2	1.0		μs	
t_{fCS}	Chip Select Pulse Fall Time	0.1	0.1	1.0	μs	
Current Ramp						
I_{OPLP}	Programming Current Linear Point		10	20	mA	Point after which the programming current ramp must rise at a linear slew rate
$I_{OP(max)}$	Output Programming Current Limit	155	160	165	mA	Apply current ramp to selected output
$V_{OP(max)}$	Output Programming Voltage Limit	24	25	26	V	
SR_{IOP}	Current Slew Rate	0.9	1.0	1.1	mA/μs	Constant after Linear Point
V_{PS}	Blow Sense Voltage	0.7			V	
t_{dBP}	Delay to Programming Ramp	2.0	3.0		μs	V_{CSP} must be at minimum
t_{LP}	Time to Reach Linear Point	0.2	1.0	10	μs	
t_{SS}	Program Sense Inhibit	2.0	3.0	10	μs	
t_{tp}	Time to Program Fuse	3.0		150	μs	
t_{hAP}	Programming Ramp Hold Time	1.4	1.5	1.6	μs	After fuse programs
t_{flOP}	Program Ramp Fall Time		0.1	0.2	μs	

Notes

1. Total time V_{CC} is on to program fuse is equal to or greater than the sum of all the specified delays, pulse widths and rise/fall times.
2. t_{OFF} is equal to or greater than t_{ON}.
3. Rise and fall times are from 10% to 90%.
4. Recommended programming temp. $T_C = +25°C \pm 10°C$.

Isoplanar-Z TTL PROM Current-Pulse Programming Specifications

Current-Pulse Programming Timing Diagram



Current-Pulse Programming Specifications[4]

Symbol	Parameter	Min	Recommended Value	Max	Units	Comments
Power Supply						
V_{CC}	Power Supply Voltage	6.4	6.5	6.6	V	Typical I_{CC} at 6.5 V = 250 mA
t_{rVcc}	Power Supply Rise Time[3]	0.2	2.0		μs	
t_{fVcc}	Power Supply Fall Time	0.2	2.0		μs	
t_{ON}	V_{CC} On Time	(1)				See Programming Timing Diagram
t_{OFF}	V_{CC} Off Time	(2)				
	Duty Cycle for V_{CC}			50	%	$t_{ON}/(t_{OFF} + t_{ON})$

Current-Pulse Programming Specifications[4] (Cont'd)

Symbol	Parameter	Min	Recommended Value	Max	Units	Comments
Read Strobe[5]						
t_{dRBP}	Read Delay before Programming		3.0		μs	Initial Check
t_W	Fuse Read Time		1.0		μs	
t_{dVcc}	Delay to V_{CC} Off		1.0		μs	
t_{dRAP}	Delay to Read after Programming		3.0		μs	Verify
Chip Select						
V_{CSP}	Chip Select Programming Voltage	20.0	20.0	22.0	V	
I_{CSP}	Chip Select Program Current Limit	175	180	185	mA	
V_{IL}	Input Voltage LOW	0	0	0.4	V	
V_{IH}	Input Voltage HIGH	2.4	5.0	5.0	V	
t_{dCS}	Delay to Chip Deselect		1.0		μs	
t_{rCS}	Chip Select Pulse Rise Time	3.0	4.0		μs	
t_{dAP}	Delay to Chip Select Time	0.2	1.0		μs	
t_{fCS}	Chip Select Pulse Fall Time	0.1	0.1	1.0	μs	
Programming Current-Pulse Train						
I_{IOP}	Initial Current Pulse		40.0	40.0	mA	80 mA may be applied when programming the 93Z564/93Z565
$I_{OP(max)}$	Output Programming Current Limit	155	160	165	mA	Apply current pulse to selected output
$V_{OP(max)}$	Output Programming Voltage Limit	24	25	26	V	
t_{RIOP}	Programming Pulse Rise Time	160	100	100	mA/μs	
t_{dBP}	Delay to Initial Programming Pulse	2.0	3.0		μs	V_{CSP} must be at minimum
t_{PW}	Programming Pulse Widths	8.0	9.0	10.0	μs	
t_{fIOP}	Programming Pulse Fall Time[3]	0.1	0.1	.02	μs	
ΔI_{OP}	Current Pulse Step Increase	5.0	10.0	10.0	mA	
	Duty Cycle for Programming Pulses	10	50	50	%	Each successive pulse is increased by I_{OP}

Notes

1. Total time V_{CC} is on to program fuse is equal to or greater than the sum of all the specified delays, pulse widths and rise/fall times.
2. t_{OFF} is equal to or greater than t_{ON}.
3. Rise and fall times are from 10% to 90%.
4. Recommended programming temp. $T_C = +25°C \pm 10°C$.
5. Proceed to next address after read strobe indicates programmed cell.

7

Notes

FAIRCHILD
A Schlumberger Company

93Z458/93Z459
16 x 48 x 8 Field Programmable Logic Array

Memory and High Speed Logic

Description

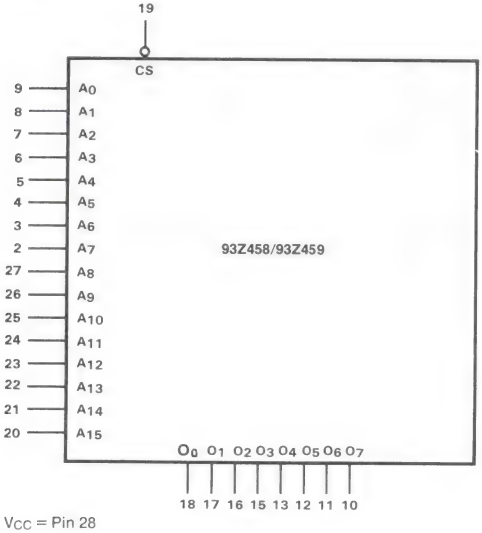
The 93Z458 and 93Z459 are bipolar Field Programmable Logic Arrays (FPLAs) organized with 16 inputs, 48 product terms and eight outputs. The 16 inputs and their complements can be fuse linked to the inputs of 48 AND gates (48 product terms). Each of the 48 AND gates can be fuse linked to eight 48-input OR gates (eight summing terms). Each output may be programmed active HIGH or active LOW. The devices are identical except for the output stage. The 93Z458 has open-collector outputs; the 93Z459 has three-state outputs. In either case, the outputs are enabled when CS is LOW.

- **Commercial Address Access Time — 45 ns Max**
- **Military Address Access Time — 65 ns Max**
- **Fully Programmable Product Array, Summing Array and Output Polarity**
- **Available with Open collector (93Z458) or Three State (93Z459) Outputs**

Pin Names

$\overline{A_0}$–A_{15}	Address Inputs
$\overline{CS}$	Chip Select Input
O_0–O_7	Data Outputs
V_P	Programming Pin

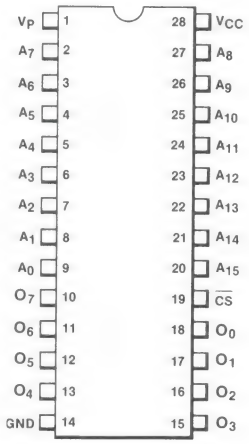
Logic Symbol



V_{CC} = Pin 28
GND = Pin 14

Connection Diagram

28-Pin DIP (Top View)

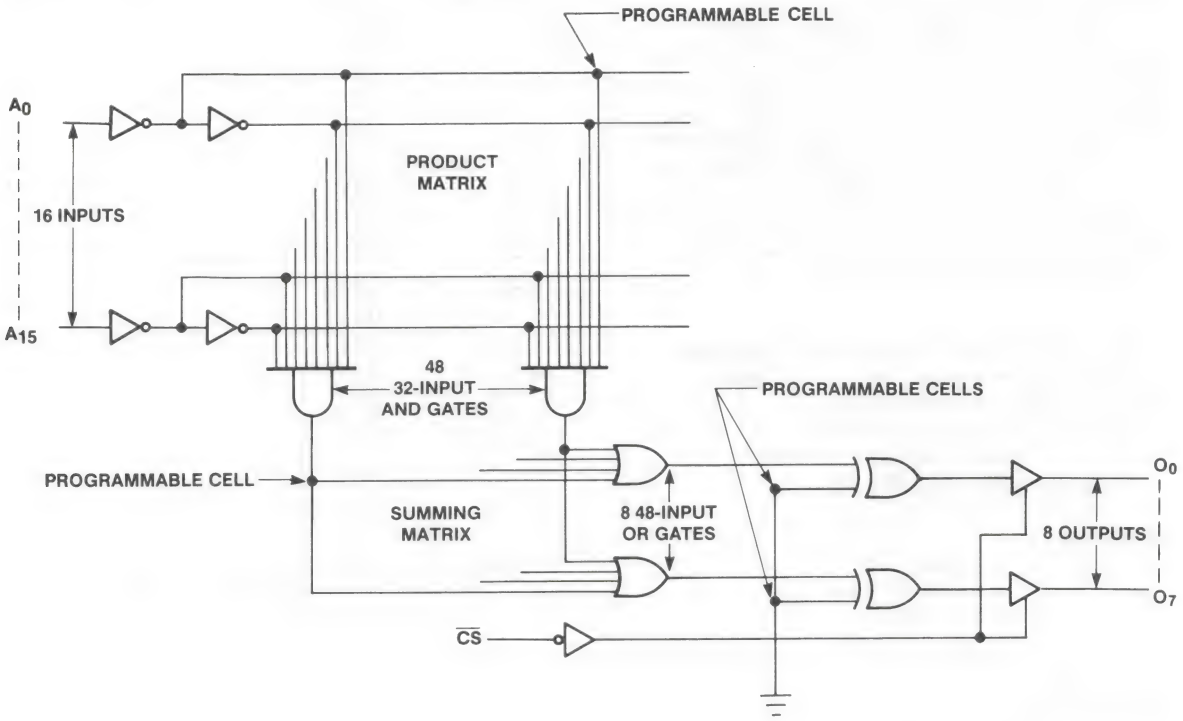


Note

The 28-pin Flatpak and the 28-pin Leadless Chip Carrier have the same pinout (Connection Diagram) as the 28-pin DIP.

8

Logic Diagram



Functional Description

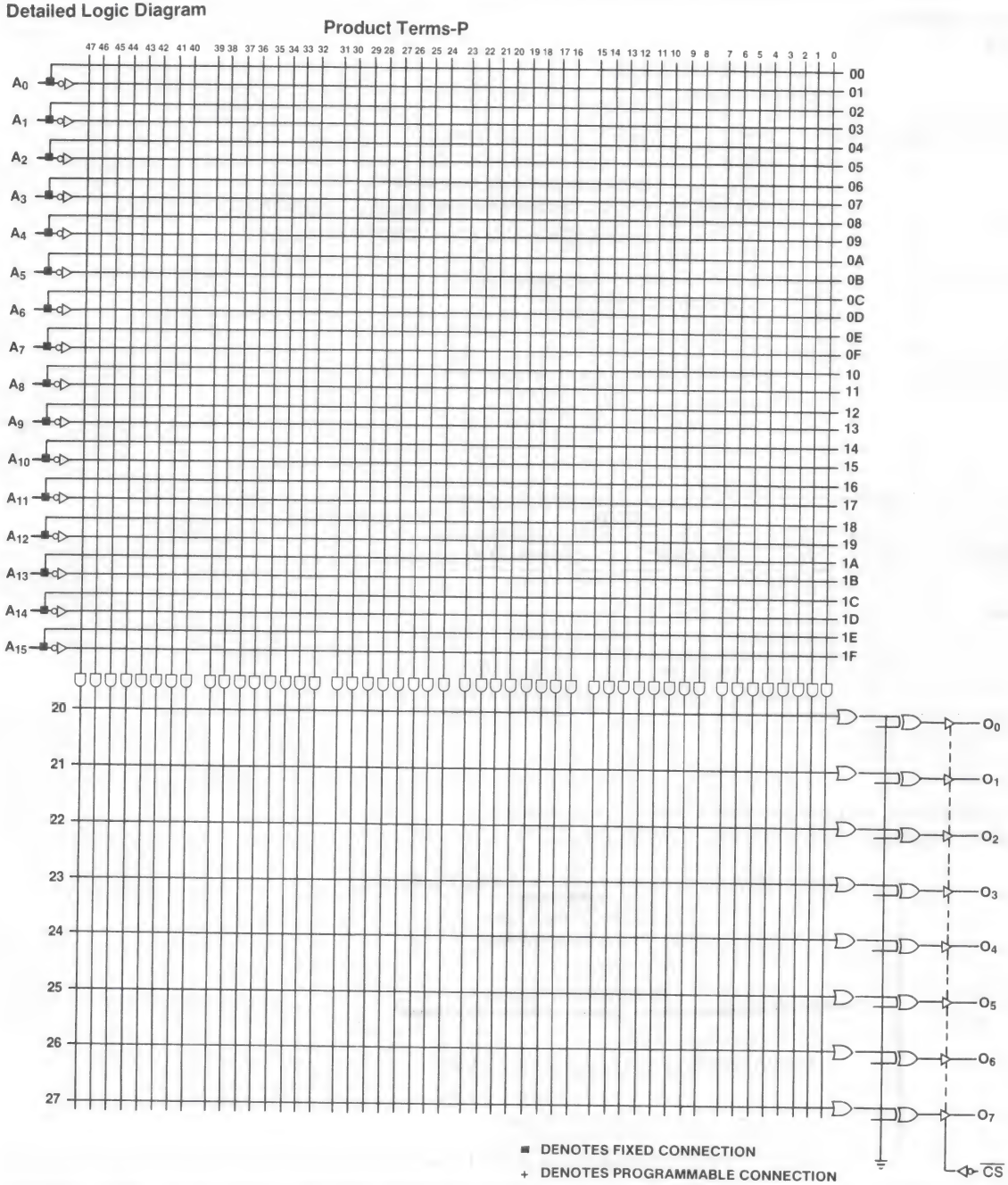
The 93Z458 and 93Z459 are bipolar Field Programmable Logic Arrays (FPLAs) organized 16 inputs by 48 product terms by eight outputs. Open-Collector outputs are provided on the 93Z458 for use in wired-OR systems. The 93Z459 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled. Chip Select for both devices is active LOW, i.e., a HIGH (logic "1") on the $\overline{CS}$ pin will disable all outputs.

The 93Z458 and 93Z459 both contain a test input line, two test product term lines and a test output line. These test fuses are accessed during both wafer sort and final test and used to assure high programmability and to guarantee DC parameters and AC performance.

The read function is identical to that of a conventional bipolar PLA. That is, a binary address is applied to inputs A_0 through A_{15}, the chip is selected, and the data is valid at the outputs after t_{AA}.

Programming is accomplished by following the sequence outlined in the *Programming Specifications* table.

Detailed Logic Diagram



8

Logic Relationships

Input Term

A_n — $n = 0, \ldots, 15$, one of 16 inputs

Product Term

$P_m = \pi_0^{15} (i_n A_n + j_n \overline{A_n})$ — $m = 0, \ldots, 47$, one of 48 product terms

where:

a) $i_n = j_n = 1$ (both true and false programmed)

b) $i_n \neq j_n$ for programmed input (true or false line programmed)

c) $i_n = j_n = 0$ for Don't Care input (unprogrammed input)

$F_r = \Sigma_0^{47} P_m$ — $r = 0, \ldots, 7$, the OR function of the 48 product terms

Summing Term

$S_r = \Sigma_0^{47} k_m P_m$ — where $k_m = 0$ for product term inactive

$k_m = 1$ for product term active

				Output	
Mode	$\overline{CS}$	F_r	S_r	**Active HIGH**	**Active LOW**
Read	L	H	L	L	H
	L	H	H	H	L
	L	L	X	L	H
Disable	H	X	X	H (93Z458)	H (93Z458)
	H	X	X	High-Z (93Z459)	High-Z (93Z459)

H = HIGH Voltage Levels
L = LOW Voltage Levels
X = Don't Care

By programming, the eight outputs of an FPLA can be made to relate to the 16 inputs as given by the following example:

8 outputs total

$$O_1 = A_0 \overline{A_6} A_{14} + \overline{A_2}\,\overline{A_{15}} + \underbrace{\overline{A_0} A_1 \ldots A_{15}}_{\text{One Product Term, 16 input terms max}} + \overline{A_8} A_{10} \overline{A_{13}}$$

One Output, 48 product terms max

$$O_2 = A_0 \overline{A_6} A_{14} + \overline{A_2}\,\overline{A_{15}}$$

(Output polarity programmed, active HIGH)

$$O_7 = \overline{(\overline{A_8} A_{10} \overline{A_{13}} + A_4 \overline{A_7}\,\overline{A_9} A_{11} \overline{A_{12}})}$$

(Output polarity not programmed, active LOW)

Programming

The 93Z458 and 93Z459 are delivered in an unprogrammed state, characterized by:

- **All vertical cells intact**
- **All 8 output buffers in active LOW state**
- **All outputs read HIGH**

Programming and verifying the Product Matrix, the Summing Matrix, and the Output Polarity are outlined below.

Program Product Matrix

In the initial unprogrammed state the 48 AND gates of the product matrix are not connected. Programming the vertical cell located by the selection of an input line, An, and the mth AND gate includes the input term in the logic expression for the mth AND gate. If all vertical cells were programmed, the resulting logic expression for the AND gates would be $A_0\overline{A_0}A_1\overline{A_1}...A_{15}\overline{A_{15}}$. In the unprogrammed state, the logic expression for each AND gate is "1".

- **Program one input at a time.**
- **All unused inputs of programmed product terms are not required to be programmed.**
- **Inputs of unused product lines are not required to be programmed.**
- **Pin 18 (0_0) is in the read mode (open collector). Care must be taken so that this pin is either left open, grounded, or loaded such that the current flowing into the pin does not exceed 16 mA.**

1. Connect pin 14 (GND) to ground.
2. Connect pin 28 (V_{CC}) to 6.5 V.
3. Apply TTL levels to pins 10 through 13, 15, and 16 (0_7 through 0_2) to address an on-chip 1-of-48 decoder to select the AND gate to be programmed (0_7 = LSB and 0_2 = MSB).
4. Apply +12.0 V to all input pins (A_0 through A_{15}).
5. Apply the proper TTL level to an A_n input pin as follows (program one input at a time):
   a. If the product term to be programmed contains the input term A_n (where n = 0 through 15), lower the A_n pin to a TTL LOW level.
   b. If the product term to be programmed contains the input term $\overline{A_n}$, lower the $\overline{A_n}$ to a TTL HIGH level.
6. Connect pin 19 ($\overline{CS}$) to 20V.
7. Apply a programming current ramp to pin 1 (V_p) according to the Programming Specifications table.
8. Repeat steps 4 through 7 for each input of the selected product term.
9. Repeat steps 3 through 8 for all other product terms to be programmed.

Verify Product Matrix

1. Connect pin 14 (GND) to ground.
2. Connect pin 28 (V_{CC}) to 6.5 V or 4.5 V[1].
3. Connect pin 19 ($\overline{CS}$) to a TTL HIGH level.
4. Apply TTL levels to pins 10 through13, 15, and 16 (0_7 through 0_2) to address an on-chip 1-of-48 decoder to select the product line to be read (0_7 = LSB and 0_2 = MSB).
5. Apply +12.0 V to all input pins (A_0 through A_{15}).
6. Test the state of the A_n input as follows:
   a. Lower the A_n pin to a TTL HIGH level and sense the voltage on pin 18 (0_0).
   b. Lower the A_n pin to a TTL LOW level and sense the voltage on pin 18 (0_0).
7. The state of the A_n input is determined as follows:

	A_n = TTL HIGH	A_n = TTL LOW	Condition of A_n for Selected Product Term
Level at Output 0 *(notes 2, 3,4)*	H	H	Unprogrammed
	H	L	A_n in P-Term
	L	H	$\overline{A_n}$ in P-Term
	L	L	Both A_n and $\overline{A_n}$ in P-Term

8. Repeat steps 5 through 7 for each input of the selected product term.
9. Repeat steps 4 through 8 for all other product terms.

Notes

1. When verifying each cell immediately after applying the current ramp, V_{CC} can be held at 6.5V.
   The verification cycle (blank check or pattern check) must consist of two passes, one at V_{CC} = 6.5 V, one at V_{CC} = 4.5 V.
2. 0_0 in this mode functions as an open-collector output.
3. The table above is valid regardless of the polarity (active HIGH or active LOW) of 0_0.
4. Pin 1 (V_P) should be either floating or grounded.

8

Program Summing Matrix

The inputs to the eight OR gates of the summing matrix are not connected in the unprogrammed state. Programming the vertical cell located by the selection of the mth AND gate and the nth summing line includes the product term P_m (the term programmed into the mth AND gate) in the logic expression for the nth OR gate. The nth summing line is selected by the selection of the nth output buffer where n = 0 through seven. If all the cells in the OR matrix were programmed, the resulting logic expression (sum of products) for the OR gates would be $P_0 + P_1 + P_2 ... + P_{47}$.

- **Program one output pin at a time.**
- **All unused product lines are not required to be programmed.**

1. Connect pin 14 (GND) to ground.
2. Connect pin 28 (V_{CC}) to 6.5 V.
3. Apply TTL levels to pins 4 through 9 (A_5 through A_0) to address an on-chip 1-of-48 decoder to select the AND gate to be programmed (A_0 = LSB and A_5 = MSB).
4. Apply TTL HIGH level to pins 20 and 21 (A_{15} and A_{14}).
5. Connect the remaining input pins to + 12.0 V.
6. Connect pin 19 ($\overline{CS}$) to 20 V.
7. Apply a current ramp (see Programming Specifications table) at the pin of the output to be programmed. Other output pins should be either left open or tied to a TTL HIGH level.
8. Repeat for all outputs that are to be programmed.

Verify Summing Matrix

1. Connect pin 14 (GND) to ground.
2. Connect pin 28 (V_{CC}) to 6.5 V or 4.5 V.
3. Connect pin 19 ($\overline{CS}$) to TTL LOW level.
4. Apply TTL levels to pins 4 through 9 (A_5 through A_0) to address an on-chip 1-of-48 decoder to select the AND gate to be verified (A_0 = LSB and A_5 = MSB).
5. Apply a TTL HIGH level to pins 20 and 22 (A_{15} and A_{13}).
6. Connect the remaining input pins to +12.0 V.
7. Sense the voltage on the output pin to be verified. The programming of the selected product line to the output line can be determined as follows:

Output Reads (Note)	Vertical Cell
L	Unprogrammed (inactive)
H	Programmed (active)

Note
The condition of the vertical cell can be determined from the table above regardless of the polarity (active HIGH or active LOW) of the output buffer being verified.

8. Repeat step 7 for all outputs to be verified.
9. Repeat for all product terms programmed.

Program Output Polarity

The initial unprogrammed state of all eight output buffers is active LOW or inverting. To program an output buffer into the active HIGH or non-inverting state, follow the steps shown below:

- **Program one output at a time.**

1. Connect pin 14 (GND) to ground.
2. Connect pin 28 (V_{CC}) to 6.5 V.
3. Apply a TTL HIGH level to pins 4 through 9 (A_5 through A_0).
4. Apply a TTL HIGH level to pin 20 (A_{15}).
5. Connect the remaining input pins to +12.0 V.
6. Connect pin 19 ($\overline{CS}$) to 20V.
7. Apply a programming current ramp (see Programming Specifications table) to the pin of the output to be programmed. Other output pins should be either left open or tied to a TTL HIGH level.

Verify Output Polarity

1. Connect pin 14 (GND) to ground.
2. Connect pin 28 (V_{CC}) to 6.5 V or 4.5 V.
3. Connect pin 19 ($\overline{CS}$) to a TTL LOW level.
4. Apply a TTL HIGH level to pins 4 through 9 (A_5 through A_0).
5. Apply a TTL HIGH level to pins 21 and 22 (A_{14} and A_{13}).
6. Connect the remaining input pins to + 12.0 V.
7. Sense the voltage on the pin of the output buffer to be verified. The condition of the output can be determined as follows:

Output Reads	Output State
H	Active LOW
L	Active HIGH

8. Repeat step 7 with V_{CC} at the LOW V_{CC} Read recommended value.

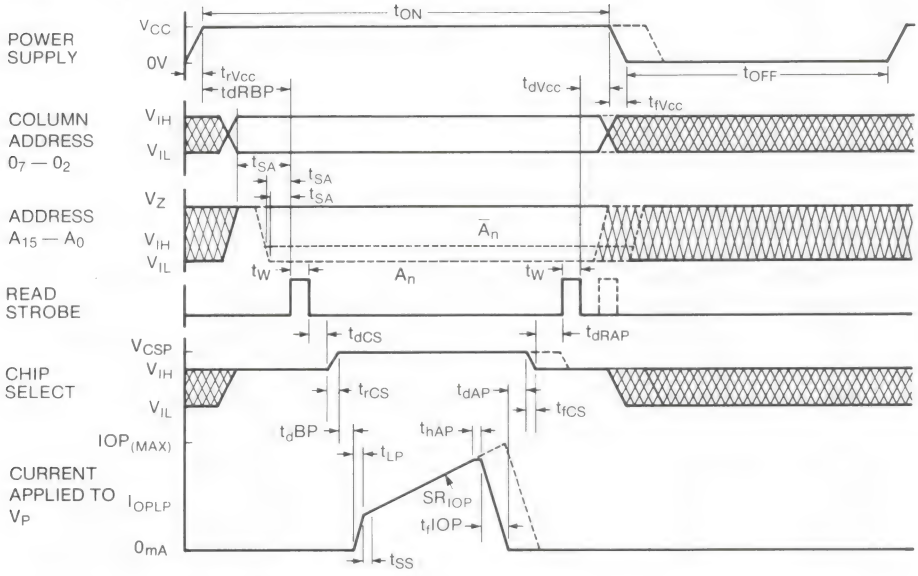
The table given below summarizes the full programming and verifying procedures.

Summary of Pin Voltages (Volts)

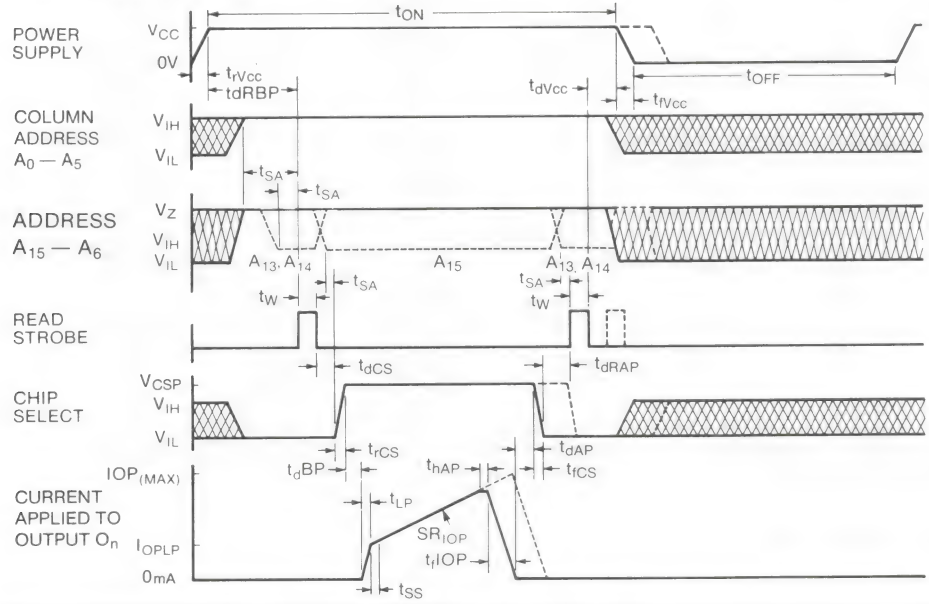
	Read	Program Product Matrix	Verify Product Matrix	Program Summing Matrix	Verify Summing Matrix	Program Output Polarity	Verify Output Polarity
Pin 1 (V_P)	***	*****	***	***	***	***	***
Pin 2 (A_7)	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 3 (A_6)	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 4 (A_5)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 5 (A_4)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 6 (A_3)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 7 (A_2)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 8 (A_1)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 9 (A_0)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 10 (O_7)	READ	TTL	TTL	****	READ	****	READ
Pin 11 (O_6)	READ	TTL	TTL	****	READ	****	READ
Pin 12 (O_5)	READ	TTL	TTL	****	READ	****	READ
Pin 13 (O_4)	READ	TTL	TTL	****	READ	****	READ
Pin 14 (GND)	GND	GND	GND	GND	GND	GND	GND
Pin 15 (O_3)	READ	TTL	TTL	****	READ	****	READ
Pin 16 (O_2)	READ	TTL	TTL	****	READ	****	READ
Pin 17 (O_1)	READ	**	**	****	READ	****	READ
Pin 18 ($\overline{O_0}$)	READ		READ	****	READ	****	READ
Pin 19 ($\overline{CS}$)	TTL LOW	20.0	TTL HIGH	20.0	TTL LOW	20.0	TTL LOW
Pin 20 (A_{15})	TTL	12.0*	12.0*	TTL HIGH	TTL HIGH	TTL HIGH	12.0
Pin 21 (A_{14})	TTL	12.0*	12.0*	TTL HIGH	12.0	12.0	TTL HIGH
Pin 22 (A_{13})	TTL	12.0*	12.0*	12.0	TTL HIGH	12.0	TTL HIGH
Pin 23 (A_{12})	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 24 (A_{11})	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 25 (A_{10})	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 26 (A_9)	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 27 (A_8)	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 28 (V_{CC})	5.0	6.5	6.5	6.5	6.5	6.5	6.5

*For selection of input apply TTL HIGH or TTL LOW
**Left open or TTL HIGH
***Left open or grounded
****Left open, TTL HIGH, or programming current ramp
*****Programming current ramp

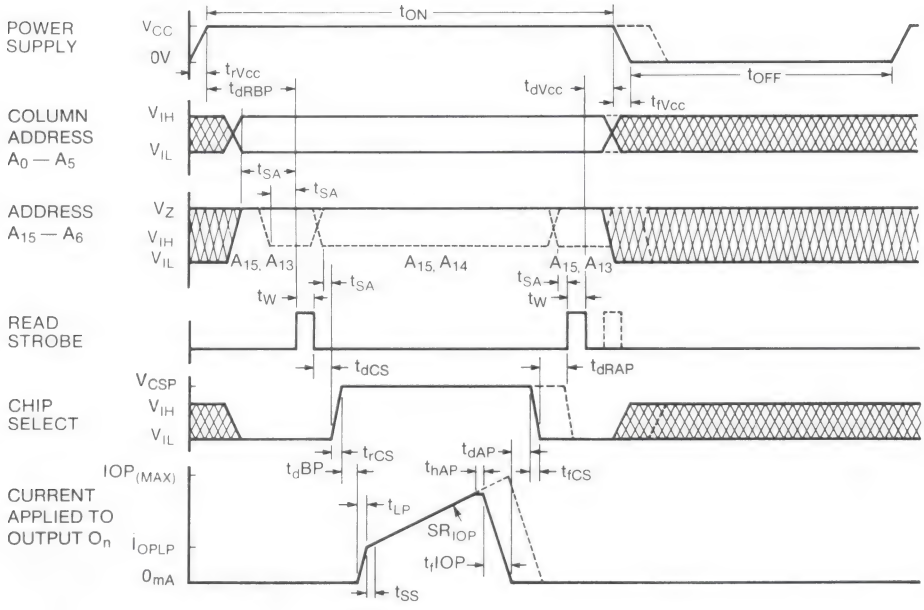
Product Matrix
Programming Timing Diagram



Output Polarity
Programming Timing Diagram



Summing Matrix
Programming Timing Diagram



Note: Current Pulse programming may be used in place of Current Ramp programming. See pages 7-20 and 7-21

8

Programming Specifications(4)

Symbol	Parameter	Min	Recommended Value	Max	Units	Comments
Power Supply						
V_{CC}	Power Supply Voltage	6.4	6.5	6.6	V	Typical I_{CC} at 6.5 V = 250 mA
t_{rVcc}	Power Supply Rise Time(3)	0.2	2.0		μs	
t_{fVcc}	Power Supply Fall Time	0.2	2.0		μs	
t_{ON}	V_{CC} On Time	(1)				See Programming Timing Diagram
t_{OFF}	V_{CC} Off Time	(2)				
	Duty Cycle for V_{CC}			50	%	$t_{ON}/(t_{OFF} + t_{ON})$

Programming Specifications (4) (Cont'd)

Symbol	Parameter	Min	Recommended Value	Max	Units	Comments
Read Strobe						
t_{dRBP}	Read Delay before Programming		3.0		μs	Initial Check
t_w	Fuse Read Time		1.0		μs	
t_{dVcc}	Delay to V_{CC} Off		1.0		μs	
t_{dRAP}	Delay to Read after Programming		3.0		μs	Verify
V_Z	Input Level during Program & Verify	11.0	12.0	12.0	V	
Chip Select						
V_{CSP}	Chip Select Programming Voltage	19.5	20.0	20.5	V	
I_{CSP}	Chip Select Program Current Limit	175	180	185	mA	
V_{IL}	Input Voltage LOW	0	0	0.4	V	
V_{IH}	Input Voltage High	2.4	5.0	5.0	V	
t_{dCS}	Delay to Chip Deselect		1.0		μs	
t_{rCS}	Chip Select Pulse Rise Time	3.0	4.0		μs	
t_{dAP}	Delay to Chip Select Time	0.2	1.0		μs	
t_{fCS}	Chip Select Pulse Fall Time	0.1	0.1	1.0	μs	
Current Ramp						
I_{OPLP}	Programming Current Linear Point		10	20	mA	Point after which the programming current ramp must rise at a linear slew rate
$I_{OP(max)}$	Output Programming Current Point	155	160	165	mA	Apply current ramp to selected output
$V_{OP(max)}$	Output Programming Voltage Limit	24	25	26	V	
SR_{IOP}	Current Slew Rate	0.9	1.0	1.1	mA/μs	Constant after Linear Point
V_{PS}	Blow Sense Voltage	0.7			V	
t_{dBP}	Delay to Programming Ramp	2.0	3.0		μs	V_{CSP} must be at minimum specification
t_{LP}	Time to Reach Linear Point	0.2	1.0	10	μs	
t_{SS}	Program Sense Inhibit	2.0	3.0	10	μs	
t_{tP}	Time to Program Fuse	3.0		150	μs	
t_{hAP}	Programming Ramp Hold Time	1.4	1.5	1.6	μs	After fuse programs
t_{flOP}	Program Ramp Fall Time		0.1	0.2	μs	
t_{SA}	Time to Address Setup	0.3	0.5		μs	

Notes

1. Total time V_{CC} is on to program fuse is equal to or greater than the sum of all the specified delays, pulse widths and rise/fall times.
2. T_{OFF} is equal to or greater than t_{ON}.
3. Rise and fall times are from 10% to 90%.
4. Reccommended programming temp. $T_A = +25°C \pm 10°C$.

16 x 48 x 8 FPLA Program Table

This Portion to be Completed by Fairchild

Customer Name _____ CF (XXXX) _____
Purchase Order # _____ Customer Symbolized Part # _____
Fairchild Device # _____ Date Received _____
Total Number of Parts _____ Comments _____
Program Table # _____ Rev _____ Date _____

Program Table Entries						
Input Variable			Output Function		Output Active Level	
A_n	$\overline{A}_n$	Immaterial	Product Term Present in F_r	Product Term Not Present in F_r	Active HIGH	Active LOW
H	L	- (dash)	A	· (period)	H	L
Note Enter (—) for *unused* inputs of *used* P terms			**Notes** 1) Entries independent of output polarity 2) Enter (A) for *unused* outputs of *used* P terms		**Notes** 1) Polarity programmed once only 2) Enter (L) for all *unused* outputs	

Product Term*																	Active Level							
	Input Variable																							
No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Output Function*							
																	7	6	5	4	3	2	1	0
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*Input and Output fields of *unused* P-terms can be left blank

8

DC Performance Characteristics: Over guaranteed operating ranges unless otherwise noted

Symbol	Characteristic	Min	Typ(1)	Max	Unit	Condition	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IC}	Input Clamp Diode Voltage			−1.2	V	V_{CC} = Min, I_{IN} = −18 mA	
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = Min, I_{OL} = 16 mA	
V_{OH}	Output HIGH Voltage (93Z459 only)	2.4			V	V_{CC} = Min, I_{OH} = −2.0 mA	
I_{IL}	Input LOW Current		−120	−250	μA	V_{CC} = Max, V_{IL} = 0.45 V	
I_{IH}	Input HIGH Current			40	μA	V_{CC} = Max, V_{IH} = 2.4 V	
I_{OHZ}	Output Leakage Current for High Impedance State (93Z459 only)			50 −50	μA	V_{OH} = 2.4 V V_{OL} = 0.4 V	0°C to +75°C
I_{OHZ}	Output Leakage Current for High Impedance State (93Z459 only)			100 −100	μA	V_{OH} = 2.4 V V_{OL} = 0.4 V	−55°C to +125°C
I_{CEX}	Output Leakage Current (93Z458 only)			50	μA	V_{CC} = 5.25 V, V_{CEX} = 4.95 V, 0° C to +75° C Chip Deselected	
I_{CEX}	Output Leakage Current (93Z458 only)			150	μA	V_{CC} = 5.5 V, V_{CEX} = 5.2 V, −55°C to +125°C Chip Deselected	
I_{OS}	Output Short-Circuit Current (93Z459 only)	−15	−35	−90	mA	V_{CC} = Max, V_O = 0 V, Note 2	
I_{CC}	Power Supply Current			170	mA	V_{CC} = Max, Chip Selected,	
C_{IN}	Input Pin Capacitance (3)		4.0		pF	V_{CC} = 5.0 V, V_{IN} = 2.0 V, f = 1.0 MHz, $\overline{CS}$ = V_{IH}	
C_O	Output Pin Capacitance (3)		7.0		pF	V_{CC} = 5.0V, V_O = 2.0 V, f = 1.0 MHz, $\overline{CS}$ = V_{IH}	

Commercial

AC Performance Characteristics: V_{CC} = 5.0 V ± 5%, GND = 0 V, T_C = 0° C to + 75° C

Symbol	Characteristic	Max	Unit	Condition
t_{AA}	Address to Output Access Time	45	ns	See AC Output Load
t_{ACS}	Chip Select to Output Access Time	30	ns	See AC Output Load
t_{CD}	Chip Select to Output Disable Time	30	ns	See AC Output Load

Notes on following page

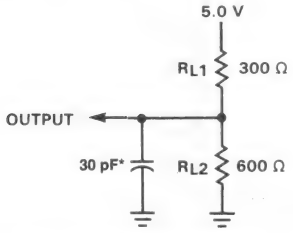
Military

AC Performance Characteristics: V_{CC} = 5.0 V ± 10%, GND = 0 V, T_C = -55°C to +125°C

Symbol	Characteristic	Max	Unit	Condition
t_{AA}	Address to Output Access Time	65	ns	See AC Test Output Load
t_{ACS}	Chip Select to Output Access Time	30	ns	See AC Test Output Load
t_{CD}	Chip Select to Output Disable Time	30	ns	See AC Test Output Load

1. Typical values are at V_{CC} = 5.0 V, T_C = +25°C and maximum loading.
2. Not more than one output to be shorted at a time. Duration of the short circuit should not exceed one second.
3. These parameters are not 100% tested, but are checked during initial design and during design changes.

Fig. 1 AC Test Loads



*Includes jig and scope capacitance

Fig. 3 Read Mode Timing

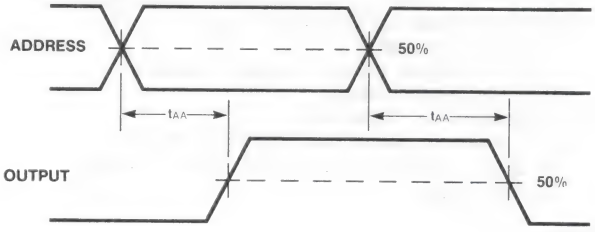
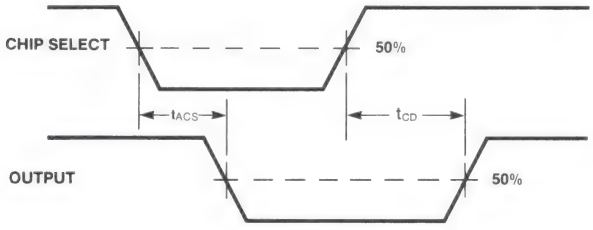
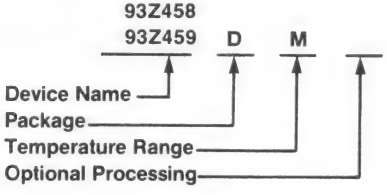


Fig. 2 Chip Select Timing



Ordering Information



Packages
- D = Ceramic DIP
- F = Flatpak
- L = Leadless Chip Carrier
- P = Plastic DIP

Temperature Ranges
- C = 0°C to +75°C
- M = −55°C to +125°C

Optional Processing
- QB = Mil Std 883 Method 5004 & 5005, Level B
- QR = Commercial Device with 160 Hour Burn In or Equivalent

8

FAIRCHILD
A Schlumberger Company

16P8B, 16RP8B, 16RP6B, 16RP4B Programmable Logic Array

Description

The FASTPLA 16P8B Series of high-performance bipolar programmable logic arrays provide 15 ns maximum propagation delays and are fully compatible with industry standard medium 20-pin PAL® devices. Designed to enhance the flexibility of the FAST family, FASTPLA 16P8B Series offers advanced architectural features including programmable output polarity, power-up reset, and power-up three-state. The devices are designed for full AC/DC testability and are manufactured with Fairchild's highly reliable Isoplanar-Z vertical-fuse technology.

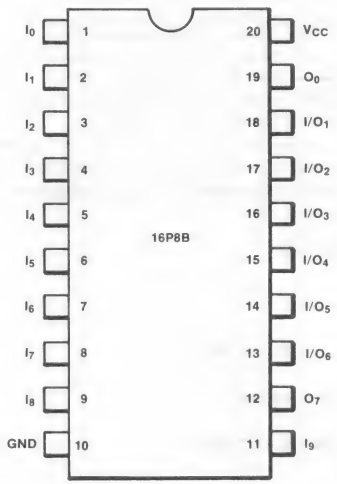
- **Extension of FAST Product Line**
- **15 ns Maximum Propagation Delays (-55°C to +125°C)**
- **180 mA Maximum I_{CC} Current**
- **Fully Compatible with Medium 20-Pin PAL® Devices**
- **Individually Programmable Output Polarity**
- **Power-Up Reset and Three-State**
- **High Programming Yields Using Highly Reliable Vertical-Fuse Technology**
- **Complete AC/DC Testability**
- **Security Fuse to Prevent Unauthorized Duplication**
- **Available in 300-mil Plastic and Ceramic DIP, Ceramic LCC, and Flatpak Packages**

Pin Names

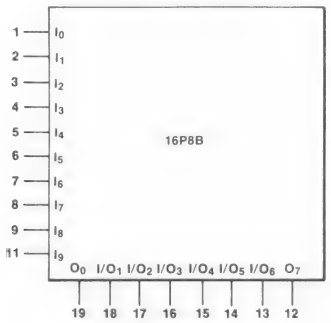
I_0 - I_9	Input
O_0, O_7	Output
I/O_1 - I/O_6	Bi-Directional Output

Connection Diagram

20-Pin DIP (Top View)



Logic Symbol



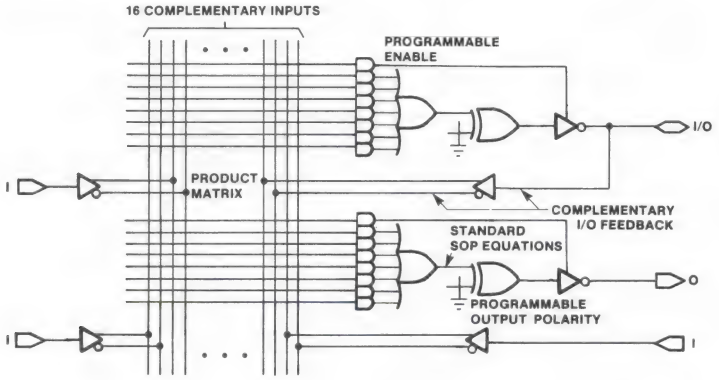
V_{CC} = pin 20
GND = pin 10

®PAL is a registered trademark of Monolithic Memories Inc.

FASTPLA 16P8B Series Summary

		16P8	16RP4	16RP6	16RP8
INPUTS	Dedicated	10	8	8	8
	Clock	—	1	1	1
LOGIC	7-Wide AND/OR	8	4	2	—
	8-Wide AND/OR	—	4	6	8
OE	Individually Programmable	8	4	2	—
	Dedicated	—	4	6	8
OUTPUTS	Programmable Polarity	8	8	8	8
	Bi-Directional	6	4	2	—
	Dedicated	2	—	—	—
	Registered (with feedback)	—	4	6	8

16P8 Functional Diagram



16P8 Functional Description

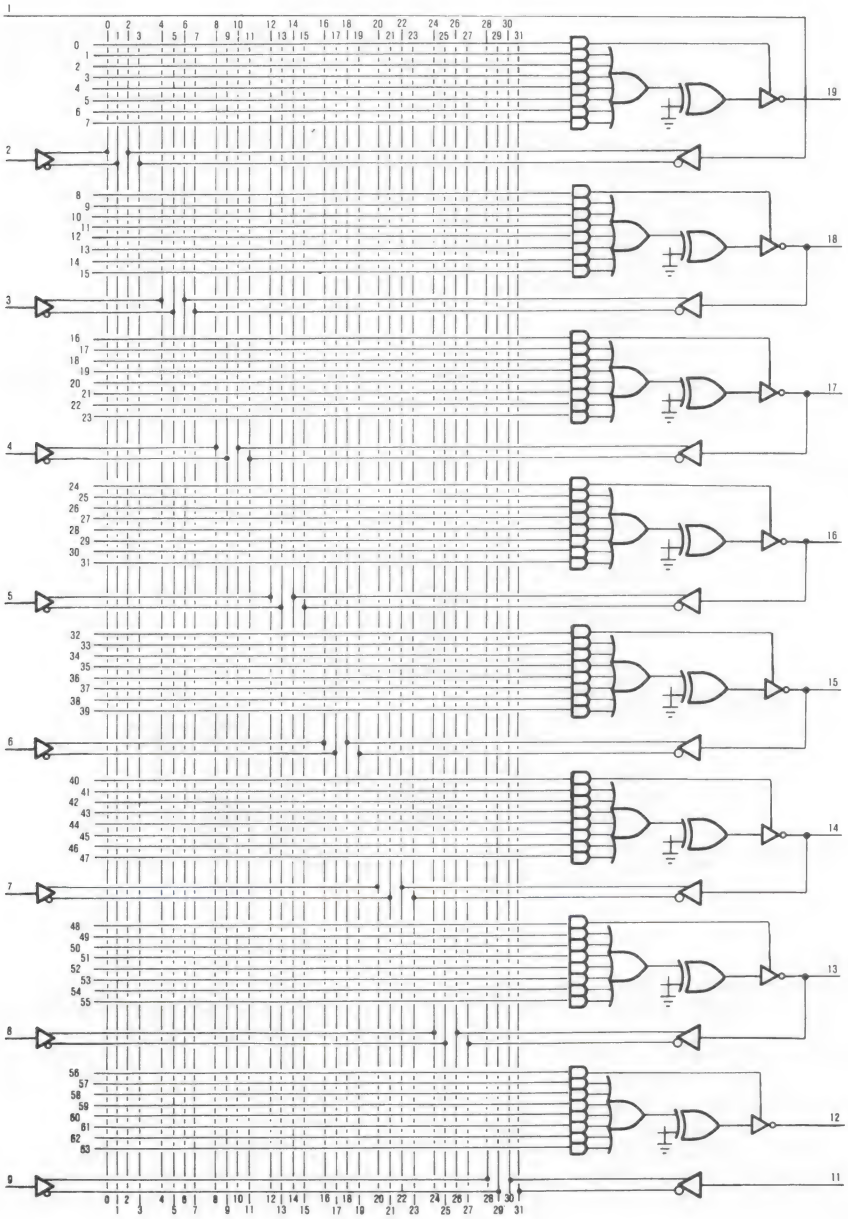
The FASTPLA 16P8B is a bipolar TTL programmable logic array (PLA) consisting of a programmable AND array feeding a fixed OR array. It is organized with 10 dedicated inputs, 2 dedicated outputs, and 6 bi-directional input/outputs as given in the family summary chart. Standard sum-of-products (SOP) form is equated at the output of the OR array as shown in the functional diagram. By use of the programmable output polarity feature, designs can be configured for 16L8 and 16H8 versions. Additionally, the output polarity can be individually programmed. Each output buffer is enabled by a dedicated active HIGH product term.

Initially all vertical fuse cells are unprogrammed. The unprogrammed output polarity fuses are equivalent to low impedance connections from the exclusive OR gate to ground. Hence, all outputs are initially active LOW. Once the polarity fuse is programmed, the output is permanently active HIGH.

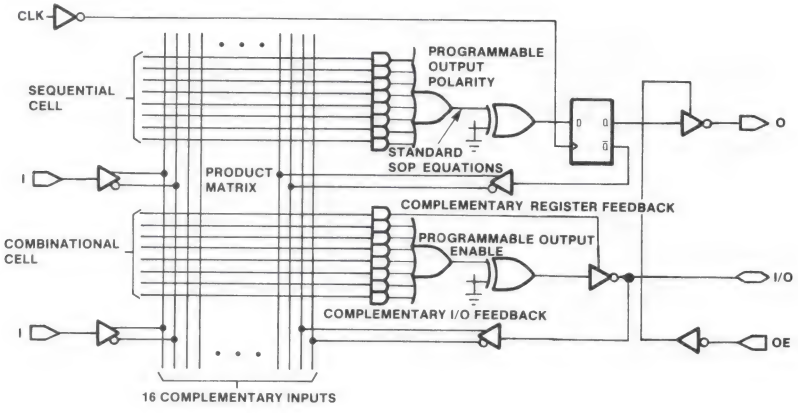
At power-on, outputs remain in the high impedance state until DC power supply conditions are met, after which they are controlled by dedicated programmable enable product terms.

C = 0° to + 75°C. Case

Logic Diagram 16P8B



16RP4, 16RP6, 16RP8 Functional Diagram



Functional Description

The FASTPLA 16RP4, 16RP6, 16RP8 are bipolar TTL programmable logic arrays (PLA) incorporating synchronous D-type registers at the output of the fixed OR array. The 16RP4, 16RP6 have both combinational output cells with feedback and programmable output enable, and sequential output cells with register feedback and dedicated output enable. The 16RP8 has eight sequential output cells with register feedback and dedicated output enable. Refer to the FASTPLA summary chart for the particulars of each device.

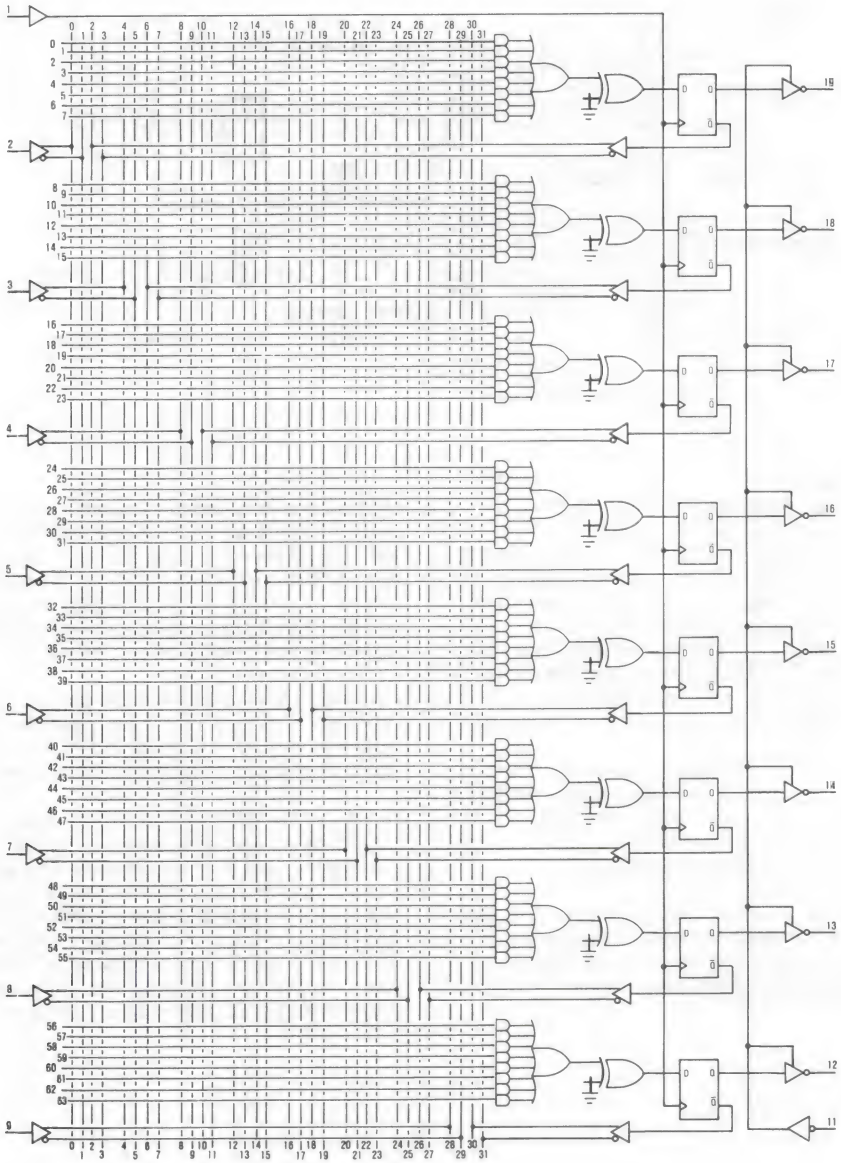
Standard sum-of-products (SOP) form is equated at the output of the OR array as shown in the functional diagram. Programmable output polarity gives the user more flexibility in design. Each output polarity may be individually defined active HIGH or active LOW.

At power-on, outputs remain in the high impedance state until DC power supply conditions are met, thereafter changing state according to the inputs (combinational cell) or output enable (sequential cell). At power on all registers are initialized to a logical LOW, thereby setting all outputs to a logical HIGH. At the first LOW-to-HIGH-transition of the clock pulse, the output state will change according to the specified D-inputs. This power-on reset feature assures the user that the registers will begin clocking from a known state and hence simplifies sequential machine design and testing.

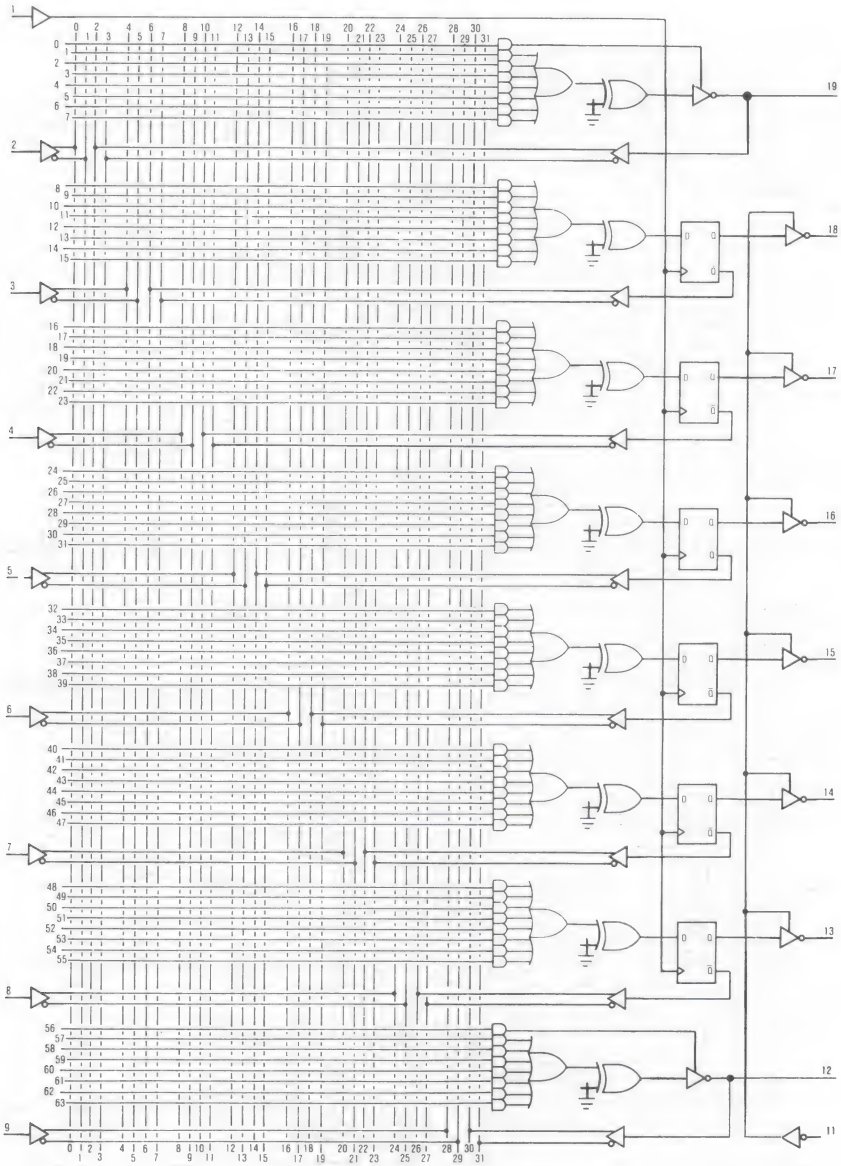
For testability, register preload is provided. It allows the user to individually preset the registers to either a HIGH or LOW level through the use of an 11 V control signal. This allows all states of a sequential design to be tested.

Initially all vertical fuse cells are unprogrammed. The outputs of the AND array are active HIGH true, thereby causing the outputs of the OR array to be HIGH true. All unprogrammed output polarity fuses are equivalent low impedance connections from the exclusive OR gate to ground. All combinational outputs read active LOW true and are enabled. Prior to the first LOW to HIGH clock transition, registered outputs read active HIGH true and are enabled according to the state of the OE pin.

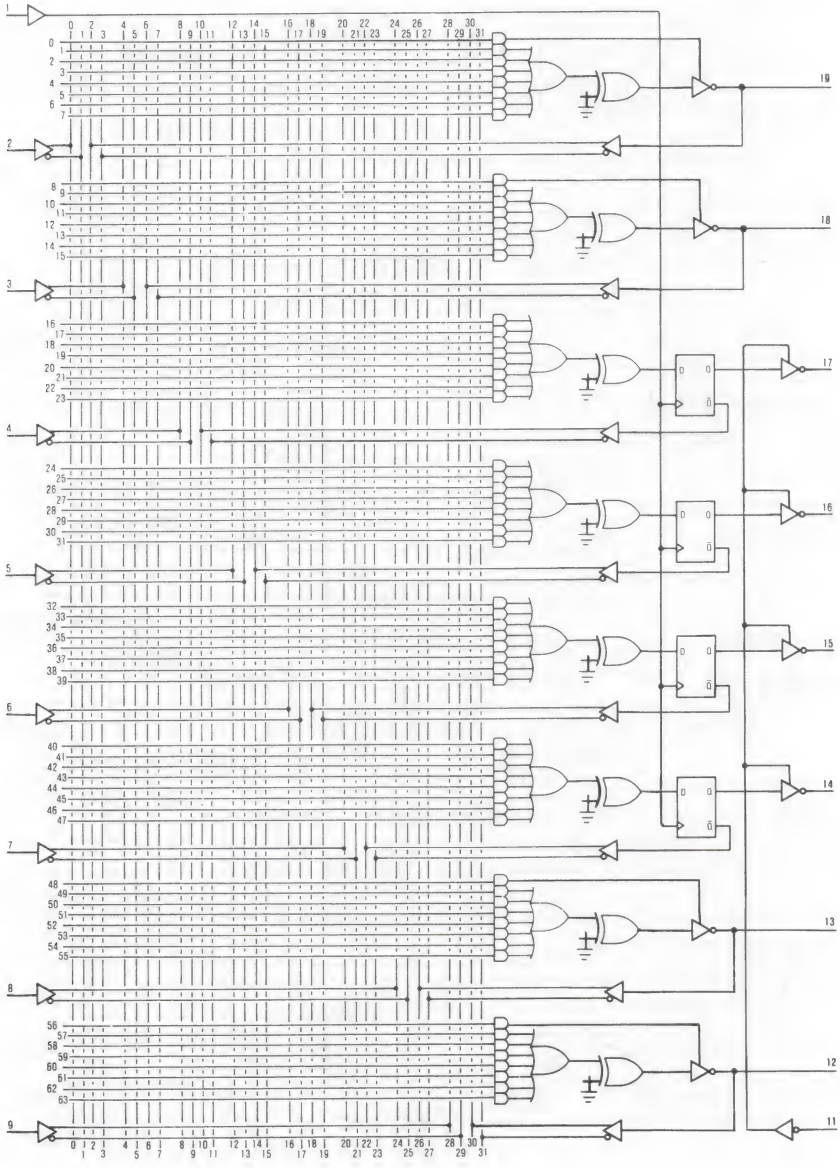
Logic Diagram 16RP8B



Logic Diagram 16RP6B



Logic Diagram 16RP4B



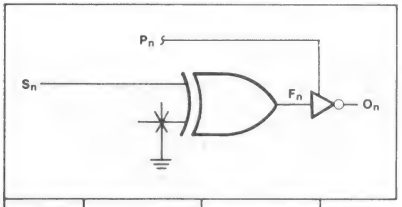
State of Delivery

- Programmability Verified
- All AND Gates are Active HIGH True
- All OR Outputs are Active HIGH True
- All Combinational Outputs are Enabled
- All Combinational Outputs are Active LOW True
- All Registered Outputs are Initialized Active HIGH True
- Security Fuse is Unprogrammed

Shown below are unprogrammed and programmed fuse map relationships:

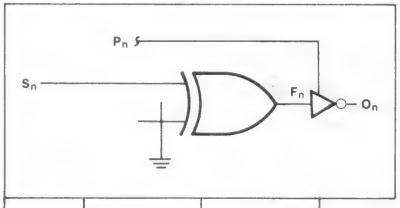
OUTPUT POLARITY

UNPROGRAMMED



O_n STATUS	F_n STATUS	CODE
ACTIVE LOW	ACTIVE HIGH	X*

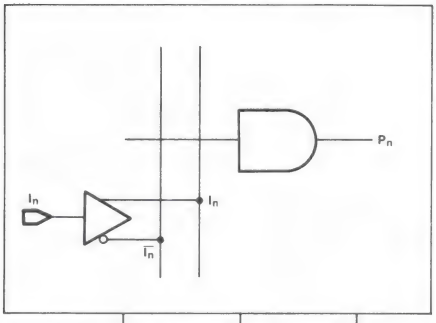
PROGRAMMED



O_n STATUS	F_n STATUS	CODE
ACTIVE HIGH	ACTIVE LOW	—

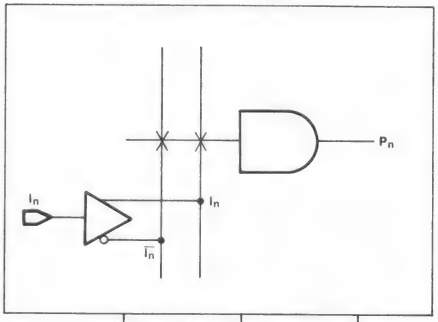
'AND' ARRAY

UNPROGRAMMED



P_n STATE	CODE
LOGIC '1'	—

PROGRAMMED



P_n STATE	CODE
LOGIC '0'	X*

S_n = SUMMING OUTPUT
P_n = PRODUCT TERM
F_n = EXCLUSIVE OR OUTPUT
I_n = INPUT VARIABLE
O_n = OUTPUT VARIBLE

* An 'X' represents a low impedance connection.

8

Absolute Maximum Rating: Above which the useful life may be impaired[1]

Storage Temperature	-65° C to +150° C
Ambient Temperature Under Bias	-55° C to +125° C
Junction Temperature Under Bias	-55° C to +150° C
V_{CC} Pin Potential to Ground Pin	-1.5 V to +7.0 V
Input Voltage [2]	-1.5 V to +7.0 V
Input Voltage Pin 1, Program Mode	-1.5 V to +21.0 V
Input Voltage Pin 11, Program Mode	-1.5 V to +12.0 V
Input Voltage Pins 2, 12-19 [7]	-1.5 V to +12.0 V
Input Current [2]	-18.0 mA to +5.0 mA
Input Current Pin 1, Program Mode	+160.0 mA
Voltage Applied to Outputs (Async)	-0.5 V to V_{CC} max. V
Voltage Applied to Outputs (Registered)	-0.5 V to V_{CC} max. V
Current Applied to Outputs	+100.0 mA

DC Performance Characteristics: Over guaranteed operating ranges unless otherwise noted

Symbol	Parameter	Min	Max	Units	V_{CC}[1]	Conditions
I_{CC}	Supply Current		180	mA	Max	All Inputs Equal 0.0 V Outputs Open
V_{IH}[2,3]	Input HIGH Voltage	2.0		V	Max	Recognized as a HIGH Signal Over Recommended V_{CC} and T_A Range
V_{IL}[2,3]	Input LOW Voltage		0.8	V	Max	Recognized as a LOW Signal Over Recommended V_{CC} and T_A Range
V_Z	Control Voltage	10.5	11.5	V	Min	
V_{CD}	Input Clamp Diode Voltage		-1.2	V	Min	I_{IN} = -18 mA
V_{OH}	Output HIGH Voltage Mil Comm	2.4 2.7		V	Min	V_{IL} = 0.0 V V_{IH} = 3.0 V I_{OH} = -3.2 mA Comm -2.0 mA Mil
V_{OL}	Output LOW Voltage		0.5	V	Min	V_{IL} = 0.0 V V_{IH} = 3.0 V I_{OL} = 24 mA Comm 20 mA Mil
I_{IH}[4]	Input HIGH Current		25	μA	Max	V_{IN} = 2.7 V
I_I[4]	Input HIGH Current		25	μA	Max	V_{IN} = 5.5 V
I_{IL}[4]	Input LOW Current		-250	μA	Max	V_{IN} = 0.5 V
I_{OZH}[4]	Output Leakage Current		50	μA	Max	V_{OUT} = 2.7 V
I_{OZL}[4]	Output Leakage Current		-50	μA	Max	V_{OUT} = 0.5 V
I_{OS}[5]	Output Short Circuit	-60	-150	mA	Max	V_{OUT} = 0.0 V
C_{IN}[6]	Input Capacitance		15	pF		V_{IN} = 2.0 V, f = 1 MHz
C_{OUT}[6]	Output Capacitance		15	pF		V_{IN} = 2.0 V, f = 1 MHz
C_{IO}[6]	Bi-Directional Pin Cap.		15	pF		V_{IN} = 2.0 V, f = 1 MHz

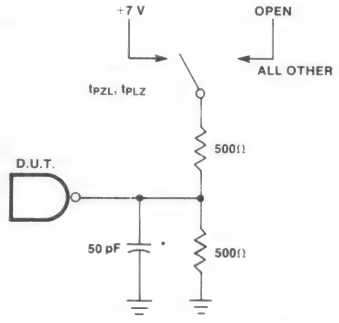
AC Performance Characteristics: $V_{CC} = 5.0\ V \pm 5\%$ (com.), $V_{CC} = 5.0\ V \pm 10\%$ (mil.), GND = 0V.

Parameter	Description	Switch[8]	Commercial		Military		Units
			Min	Max	Min	Max	
t_{PD}	Input or Feedback to Non-Registered Outputs	Open		15		15	ns
t_{PZX}[6]	Input to Output Enable ZH ZL	Open Closed		15		15	ns
t_{PXZ}[6]	Input to Output Disable HZ LZ	Open Closed		15		15	ns
t_{PZX}	Pin 11 To Output Enable ZH ZL	Open Closed		12		15	ns
t_{PXZ}	Pin 11 to Output Disable HZ LZ	Open Closed		12		15	ns
t_{CO}	Clock to Output	Open		10		10	ns
t_{SU}	Input or Feedback Setup Time		15		15		ns
t_H	Hold Time		0		0		ns
t_P	Clock Period		20		25		ns
t_{WL}[9]	Clock Width LOW		9		11		ns
t_{WH}[9]	Clock Width HIGH		8		10		ns
f_{MAX}	Maximum Clock Frequency		50		40		MHz

Performance Characteristics Notes

1. Unless otherwise restricted or extended by detail specification.
2. Either input voltage or current limit sufficient to protect inputs.
3. These are absolute values with respect to pin 10 (device ground) and includes all overshoots due to system AND/OR tester noise.
4. I/O pin leakage is the worst case of I_{OZX}, I_{IX}, X = H/L.
5. For testing I_{OS}, the use of HIGH speed test apparatus AND/OR sample and hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. For any sequence of parameter tests, I_{OS} tests should be performed last. Only one output should be shorted at a time.
6. These parameters are not 100% tested but are periodically sampled.
7. Preload/clear functions on registered outputs only. The output must be three-stated before V_Z may be applied.
8. See AC test loads.
9. $t_{WH} + t_{WL} \geq 20$ ns (com.), $t_{WH} + t_{WL} \geq 25$ ns (mil.).

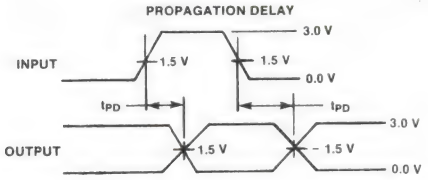
AC Test Loads

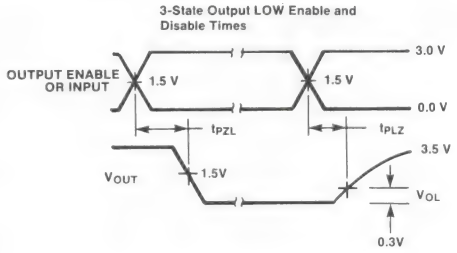


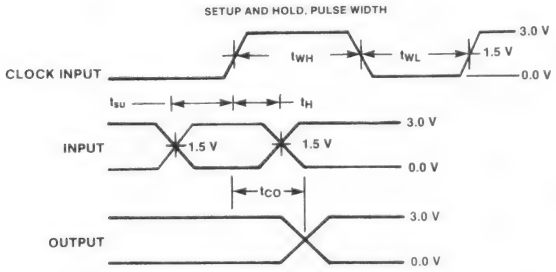
*INCLUDES JIG AND PROBE CAPACITANCE

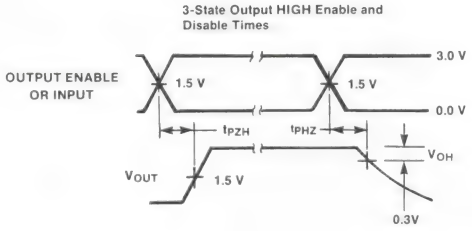
8

AC Waveforms



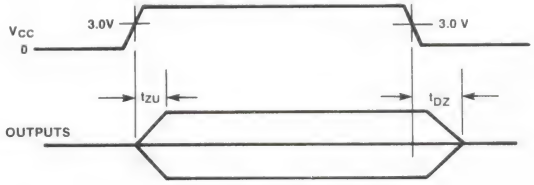






Power-up Three-state

All outputs will be disabled when V_{CC} is less than approximately 3.0V (+25°C)

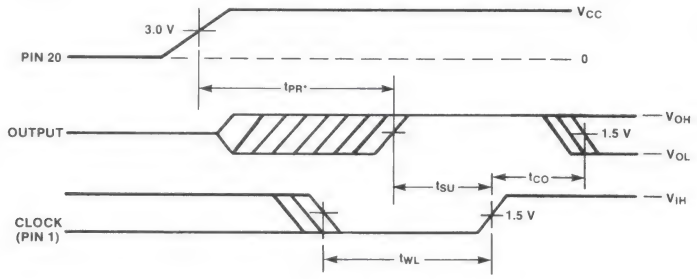


*t_{ZU} and t_{DZ} are less than 0.1 μs

Power-Up Reset

Two conditions are required to ensure a valid power-up reset:

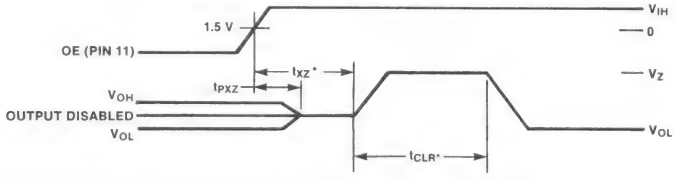
1. V_{CC} must rise to recommended DC value.
2. After reset, the clock input must be held LOW for time t_{SU} before clocking.



Preload of Registered Outputs for Testability

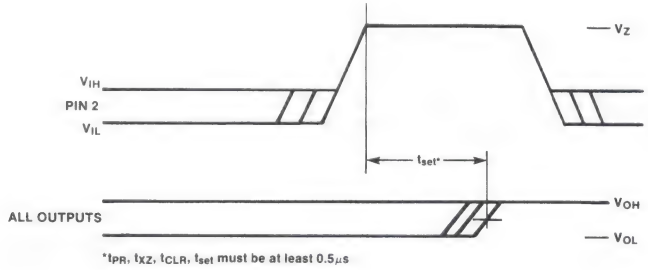
To preload a register to an active HIGH level, the following steps are required:

1. Apply a logic HIGH level voltage to the output enable input (Pin 11) to three-state the device.
2. After the specified time (t_{XZ}) raise desired output pin to the control voltage level (Vz) and hold for the specified time (t_{CLR}). (Register is set HIGH, output active LOW).



To preload all registers simultaneously to an active LOW level, the following steps are required:

1. Raise input Pin 2 to the control voltage (Vz) for the specified time (t_{set}). (All registers reset LOW, all outputs will be set active HIGH true).



*tPR, tXZ, tCLR, tset must be at least 0.5μs

Programming

The FASTPLA 16P8B Series is programmed by applying a control signal to the Edit Enable pin (pin 11) and appropriate programming waveforms to the Fusing Supply (pin 1). Individual fuses are addressed by applying TTL levels to the row and column address inputs. The Edit Output pin (pin 12 open collector output) is active HIGH when the selected fuse has been programmed.

Programming Sequence*:

1. Connect pin 10 (GND) to Ground.
2. Connect pin 20 (V_{CC}) to 5.5 V.
3. Connect pin 11 (Edit Enable) to 11 V.
4. Connect pin 12 (Edit Output) to V_{CC} through a 1-2K resistor.
5. Connect pin 1 (Fusing Supply) to fusing current source.
6. Apply TTL levels to C_0-C_6 and R_0-R_5 to address desired vertical fuse cell.
7. Apply programming current pulse train to pin 1 reading pin 12 between pulses. Terminate the pulse train when pin 12 is TTL HIGH.
8. Repeat steps 6 and 7 for the next address.

Verification Sequence*:

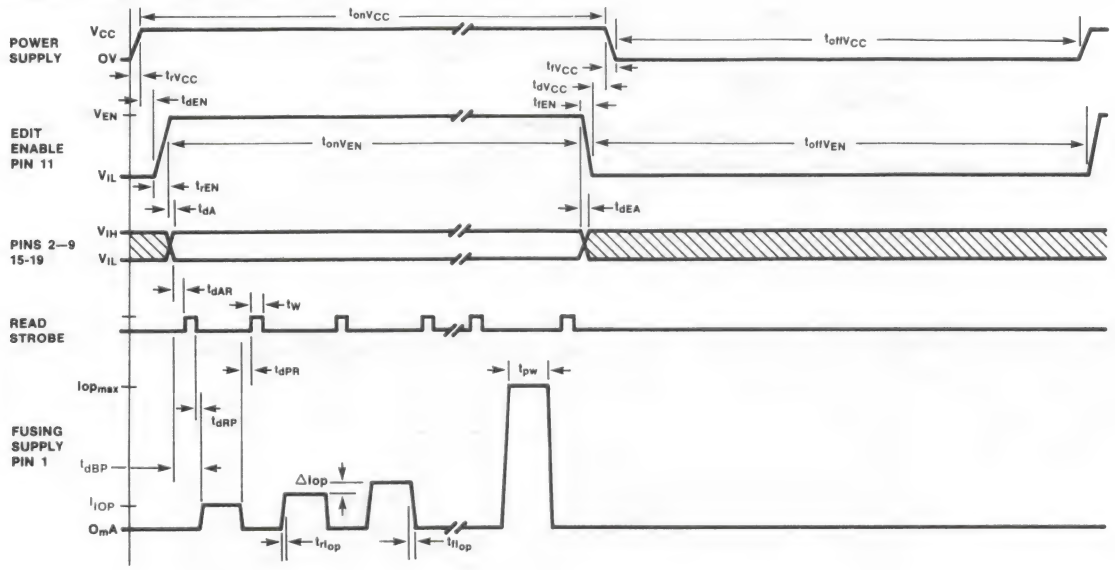
1. Connect pin 10 (GND) to Ground.
2. Connect pin 20 (V_{CC}) to 5.5 V.
3. Connect pin 11 (Edit Enable) to 11 V.
4. Connect pin 12 (Edit Output) to V_{CC} though a 1-2K resistor.
5. Apply TTL levels to C_0-C_6 and R_0-R_5.
6. Read pin 12, TTL HIGH - programmed cell.
   TTL LOW - unprogrammed cell.

*For additional information request Fairchild's complete programming algorithm specification.

Security Fuse

The security fuse is initially unprogrammed to allow editing and programming of the device. When programmed, the security fuse disables the verification circuitry on the device, thereby protecting the design from unauthorized dupication. Programming is accomplished by following the sequence as outlined in the programming specifications table.

Programming Timing Diagram



Programming Specification Notes

1. Total time V_{CC} is on to program cell is equal to or greater than the sum of all the specified delays, pulse width and rise/fall times
2. $t_{off} \geq t_{on}$
3. Rise & fall times are from 10% to 90%
4. Recommended programming temperature, t_p = +25° C ± 10°C
5. Proceed to next address after pin 12 indicates a programmed cell
6. Return to input and/or output function when address is invalid
7. Does not include rise and fall times

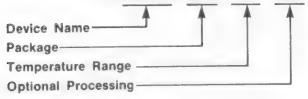
Programming Specifications[4]

Symbol	Parameter	Min	Recommended Values	Max	Units	Comments
Power Supply						
V_{CC}	Power Supply Voltage	5.4	5.5	5.6	V	
$t_{rV_{CC}}$	Power Supply Rise Time	0.2	2.0		μs	*See Note 3*
$t_{fV_{CC}}$	Power Supply Fall Time	0.2	2.0		μs	*See Note 3*
$t_{onV_{CC}}$	V_{CC} on Time[1]					*See Programming Timing Diagram*
$t_{offV_{CC}}$	V_{CC} off Time[2]					
	Duty Cycle for V_{CC}			50%		$t_{on}/(t_{on} + t_{off})$
Edit Enable Power Supply						
V_{EN}	Edit Enable Supply Voltage	10.5	11.0	11.5	V	Applied to Pin 11
t_{dEN}	Delay to Enable	1.0	2.0		μs	V_{CC} Settling Time
t_{rEN}	Enable Rise Time	0.4	2.0		μs	*See Note 3*
t_{fEN}	Enable Fall Time	0.4	2.0		μs	*See Note 3*
t_{dA}	Delay to Address	0.1	1.0		μs	Delay from 90% of V_{EN} until Addresses are Valid [6]
t_{dEA}	Delay to Address Invalid			1.0	μs	Delay from 90% of V_{EN} until Addresses are Invalid[6]
$t_{dV_{CC}}$	Delay to V_{CC} off	1.0	2.0		μs	
t_{onEN}	V_{EN} on Time					*See Programming Timing Diagram*
t_{offEN}	V_{EN} off Time					
	Duty Cycle for V_{EN}			50%		$t_{on}/(t_{on} + t_{off})$
V_{IL}		0	0	0.4	V	
V_{IH}		2.4	5.0	5.0	V	
Read Strobe [5]						
t_{dAR}	Delay from Valid Address to to Valid Read	0.1	0.5		μs	Initial Check
t_{dRP}	Delay from Read to Programming Pulse	0.1			μs	
t_{dPR}	Delay from Programming Pulse to Read	2.0			μs	Verify
t_w	Cell Read Time		1.0		μs	
Programming Current Pulse Train						
I_{lop}	Initial Current Pulse	40	40	60	mA	Current on Pin 1
I_{opmax}	Prog. Current Limit	140	140	160	mA	Current on Pin 1
V_{opmax}	Prog. Voltage Limit	19	20	20	V	Voltage on Pin 1
t_{rlop}	Prog. Pulse Rise Time	0.3	1.0	1.45	μs	*See Note 3*
t_{flop}	Prog. Pulse Fall Time		0.1	0.5	μs	*See Note 3*
t_{dBP}	Delay to I_{lop}	2	3		μs	Delay from Address Valid
t_{pw}	Pulse Width	6	7	8	μs	*See Note 7*
I_{op}	Current Pulse Step	5	10	10	mA	Each Successive Pulse is Increased by Delta I_{op}
	Duty Cycle for Prog. Pulse	10	50	50	%	

See Notes on Page 15

Ordering Information

F16P8B
F16RP4B
F16RP6B
F16RP8B SD M QB



Packages

SD = Slim Ceramic DIP
F = Flatpak
L = Leadless Chip Carrier
SP = Slim Plastic DIP

Temperature Ranges

C = 0°C to +75°C
M = -55°C to +125°C

Optional Processing

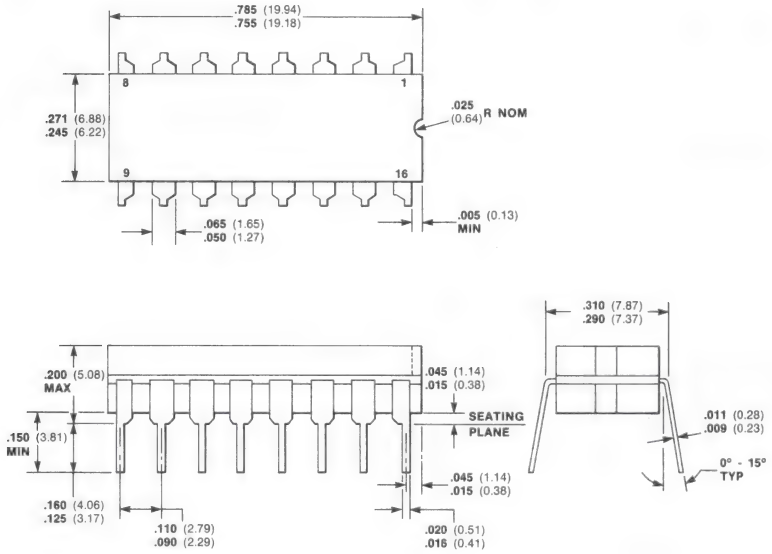
QB = Mil Std 883
Method 5004 & 5005, Level B
QR = Commercial Device with
160 Hour Burn in

Notes

Notes

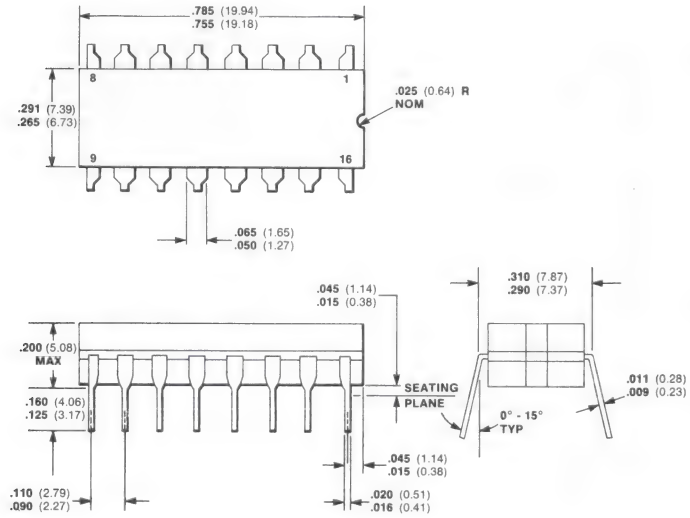
Part Number	Side-Brazed	Cerdip	Plastic DIP	Leadless Chip Carrier	Cerpak
ECL RAMs					
F100145	—	6Y	—	—	4V
F100402	—	4J	—	—	3L
F100415	—	6D	—	—	3L
F100422	—	6Y	—	—	4V
F100474	—	SH	—	—	SI
F10145A	—	4J	—	—	3L
F10402	—	4J	—	—	3L
F10415	—	6D	—	—	3L
F10422	—	6Y	—	—	4V
F10474	—	SH	—	—	SI
TTL RAMs					
93415	—	6D	9B	—	3L
93L415	—	6D	9B	—	3L
93422	—	6S	4K	2I	4P
93L422	—	6S	4K	2I	4P
93425	—	6D	9B	—	3L
93L425	—	6D	9B	—	3L
93425H	—	6D	9B	—	3L
93479	—	6S	—	—	—
MOS Static RAMs					
F1600	MB	—	RB	MC	—
F1601	MB	—	RA, RB	MC	—
ECL PROMs					
F100Z416	—	6D	—	—	3L
F10Z416	—	6D	—	—	3L
TTL PROMs					
93Z450	—	7L, 4H	9N	2J	4P
93Z451	—	7L, 4H	9N	2J	4P
93Z510	—	7L, 4H	9N	1J	4X
93Z511	—	7L, 4H	9N	1J	4X
93Z564	7S	—	—	1J	—
93Z565	7S	—	—	1J	—
93Z611	—	7L, 4H	RA	2J	4X
93Z667	SB	—	—	—	—
TTL Programmable Logic					
93Z458	—	8S	9Y	2J	2E
93Z459	—	8S	9Y	2J	2E
16P8B	—	4E	9Z	SE	—
16RP4B	—	4E	9Z	SE	—
16RP6B	—	4E	9Z	SE	—
16RP8B	—	4E	9Z	SE	—

4J 16-Pin Cerdip (.300)



Notes
Pins are solder or tin-plated alloy 42 or equivalent
Pins are intended for insertion in hole rows on **.300** (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board drilling dimensions should equal your practice for **.030** (0.76) inch diameter holes
Hermetically sealed alumina package
Package weight is 2.0 grams
Dimensions include glass over-run, misalignment, etc...
Minimum width **.023** on corner pins
Lead thickness and width may increase by **.003** (0.08)when lead finish is applied.

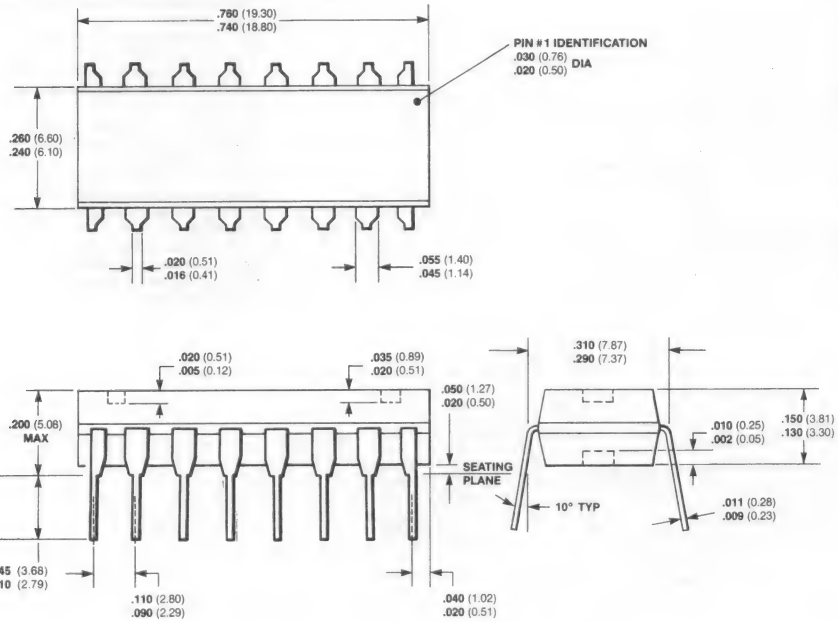
6D 16-Pin Cerdip (.300)



Notes
Pins are solder or tin-plated alloy 42 or equivalent
Pins are intended for insertion in hole rows on **.300** (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.030** (0.76) inch dia. holes
Hermetically sealed alumina package
Package weight is 2.2 grams
These dimensions include misalignment, glass over-run etc...
Lead thickness and width may increase by .003(0.08) when lead finish is applied.

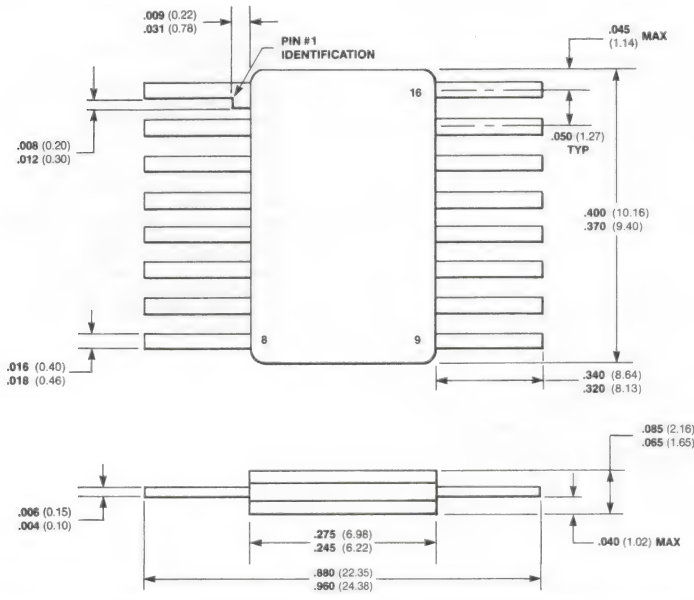
All dimensions is inches **bold** and millimeters (parentheses)

9B 16-Pin Plastic DIP (.300)



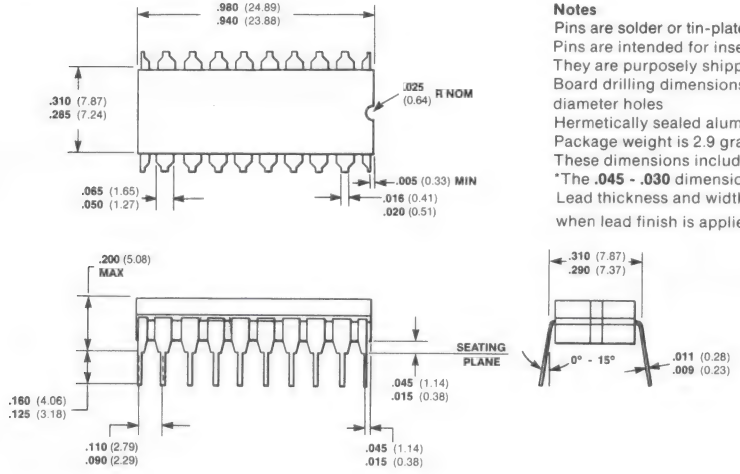
Notes
Pins are solder or tin-plated alloy 42 or equivalent
Package material is plastic
Pins are intended for insertion in hole rows on **.300** (7.63) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Package weight is 1.0 gram
Package dimensions do not include permissible flash
Lead thickness and width may increase by **.003** (0.08) when lead finish is applied

3L 16-Pin Cerpak



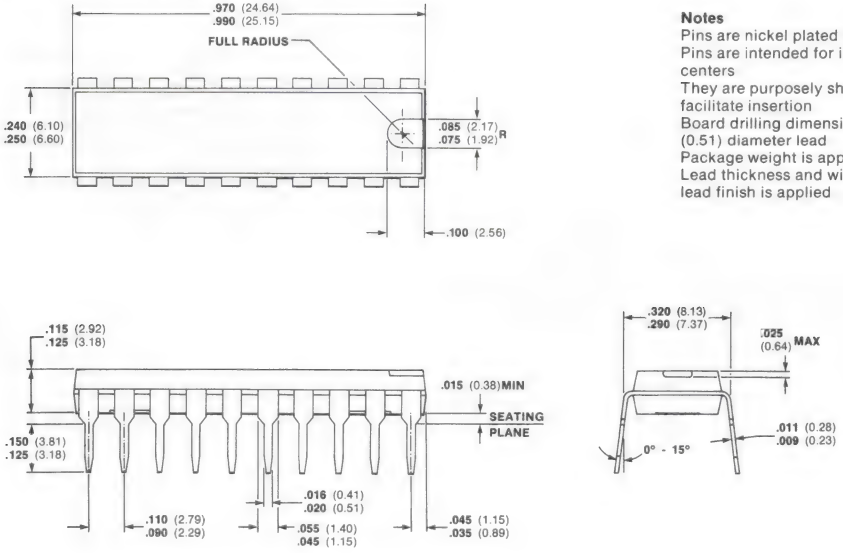
Notes
Pins are solder or tin-plated alloy 42 or equivalent
Base and cap are black alumina
Package weight is 0.5 gram
These dimensions include misalignment, glass over-run etc...
Lead thickness and width may increase by **.003** (0.08) when lead finish is applied

4E 20-Pin Cerdip (.300)



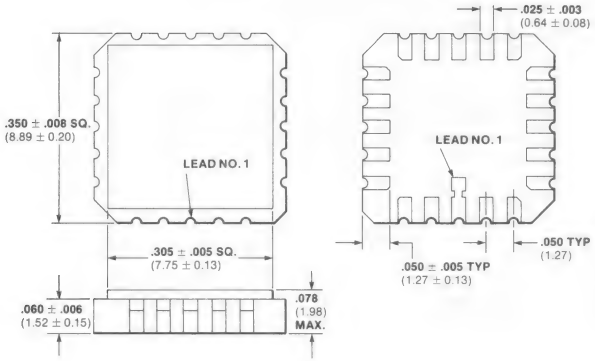
Notes
Pins are solder or tin-plated alloy 42 or equivalent
Pins are intended for insertion in hole rows on **.300** (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board drilling dimensions should equal your practice for **.030** (0.76) inch diameter holes
Hermetically sealed alumina package
Package weight is 2.9 grams
These dimensions include misalignment glass over-run etc...
*The **.045 - .030** dimension does not apply to the corner pins
Lead thickness and width may increase by **.003** (0.07) when lead finish is applied.

9Z 20-Pin Plastic DIP (.300)



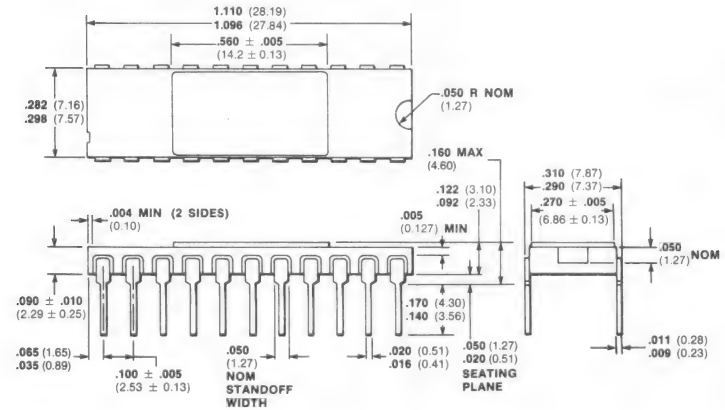
Notes
Pins are nickel plated and solder dipped copper (olin 195)
Pins are intended for insertion in hole rows on **.300** (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board drilling dimensions should equal your practice for **.020"** (0.51) diameter lead
Package weight is approximately 1.0 gram
Lead thickness and width may increase by **.003** (0.07) when lead finish is applied

SE 20-Pin Leadless Chip Carrier



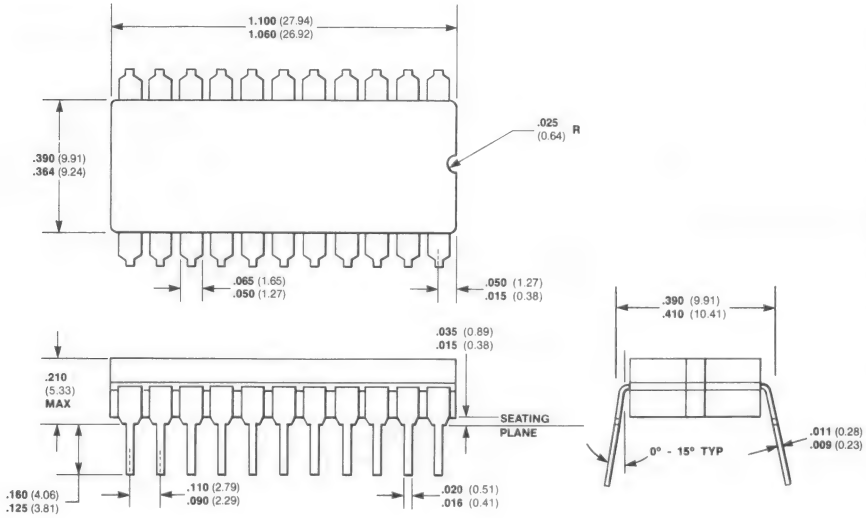
Notes
Chip carrier is 90% minimum alumina, black.
Lid is nickel/gold plated alloy 42 or equivalent.

MB 22-Pin Side-Brazed (.300)



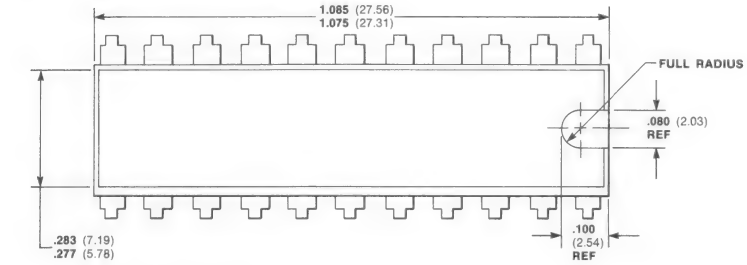
Notes
Pins are Ni/Au plated alloy 42 or equivalent.
Package material is 90% min. alumina.
Cap is Ni/Au plated kovar or equivalent.
Board drilling dimensions should equal your practice for .030(0.76) diameter holes.
Pins are intended for insertion in hole rows on .300(7.62) centers.
Pins are purposely shipped with "positive" misalignment to facilitate insertion.
Package weight is 2.05 grams.

6S/6S-S 22-Pin Cerdip (.400)

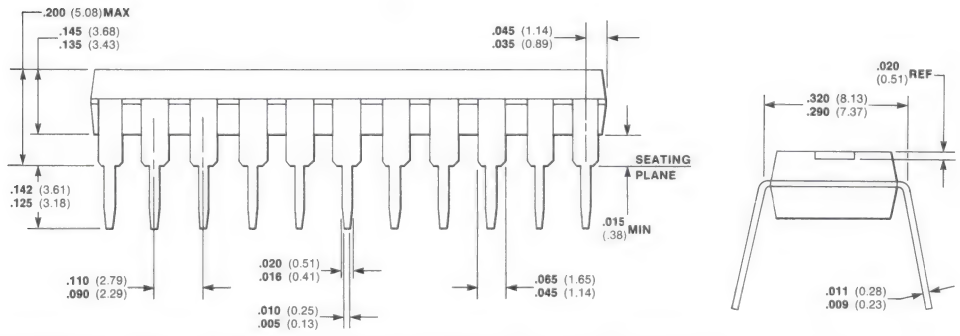


Notes
Pins are solder or tin-plated alloy 42 or equivalent
Hermetically sealed alumina package
Pins are intended for insertion in hole rows on **.400** (10.16) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Package weight is 2.2 grams
Board-drilling dimensions should equal your practice for **.030** (0.76) inch diameter holes
These dimensions include misalignment, glass over-run etc...
Lead thickness and width may increase by **.003** (0.08) when lead finish is applied.

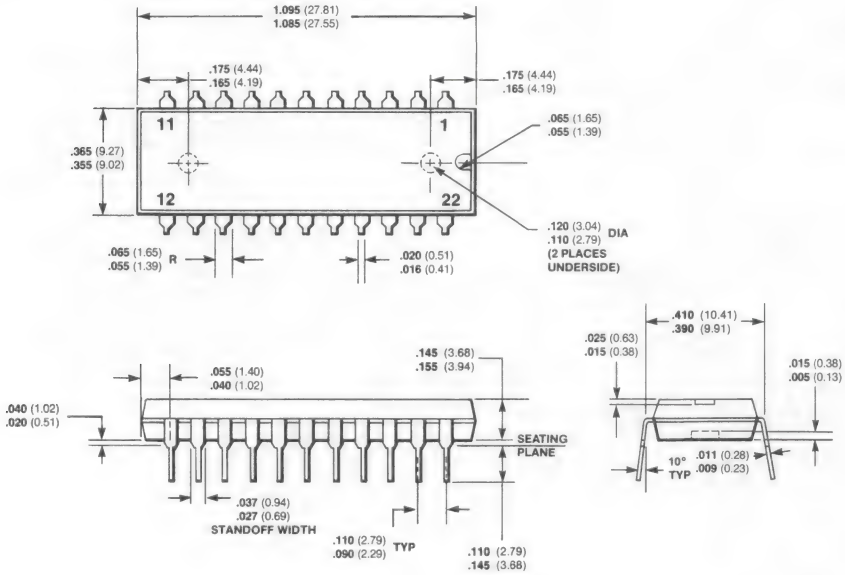
RB 22-Pin Plastic DIP (.300)



Notes
Pins are solder or tin-plated alloy 42
Pins are intended for insertion in hole rows on **.300** (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board drilling dimensions should equal your practice for **.020**" (0.51) diameter lead
Package weight is approximately 1.4 grams
Lead thickness and width may increase by **.003** (0.08) when lead finish is applied.

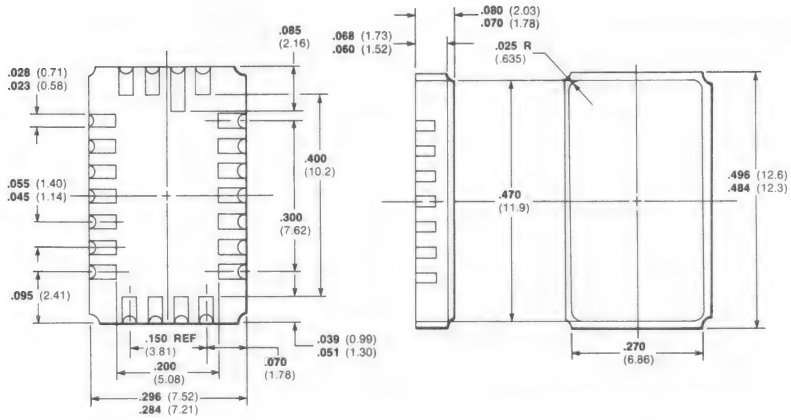


4K 22-Pin Plastic DIP (.400)



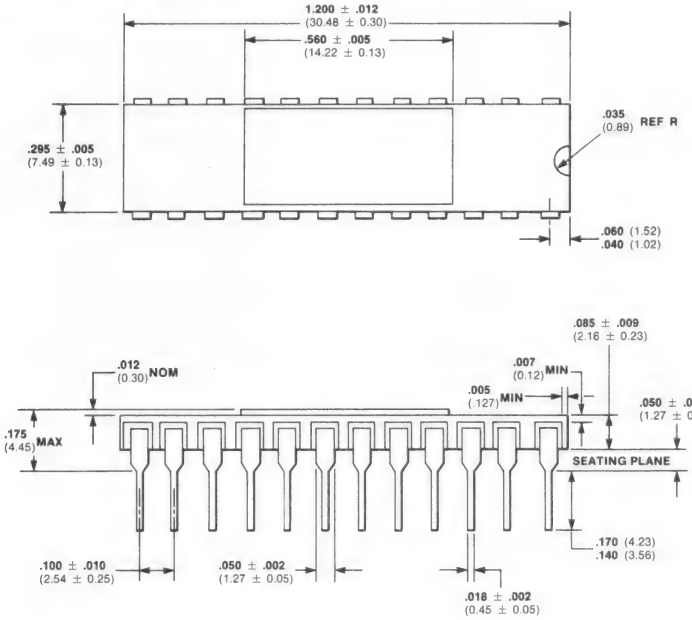
Notes
Pins are solder or tin-plated alloy 42 or equivalent
Package material is plastic
Pins are intended for insertion in hole rows on **.400** (10.16) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Package weight is 2.1 grams
Package dimensions do not include permissible flash
Lead thickness and width may increase **.003** (0.08) when lead finish is applied

MC 22-Pin Leadless Chip Carrier



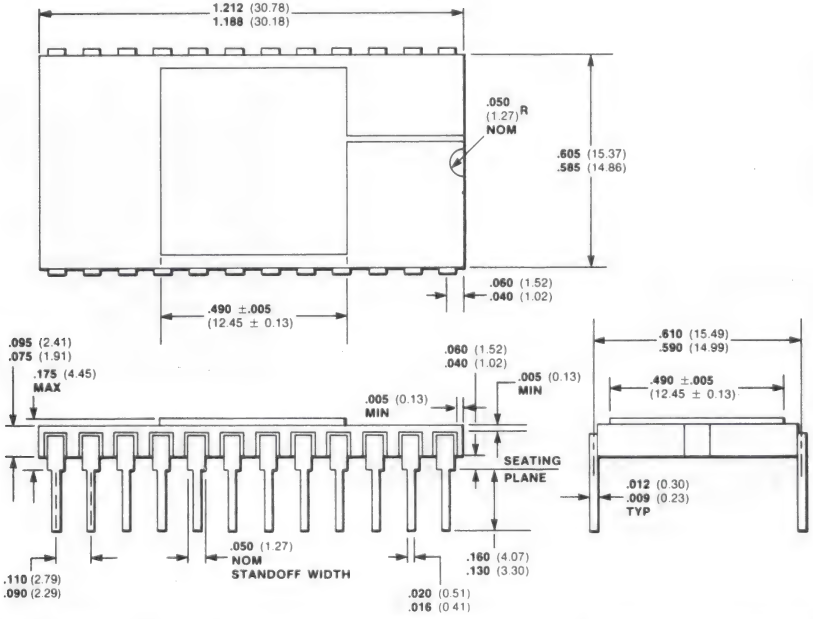
Notes
Chip carrier is 90% min. black alumina
Cap is Ni/Au plated kovar or equivalent
Cavity size is **.214 x .325** (5.44 x 8.26)
Package weight is 0.60 gram

SB 24-Pin Side-Brazed (.300)



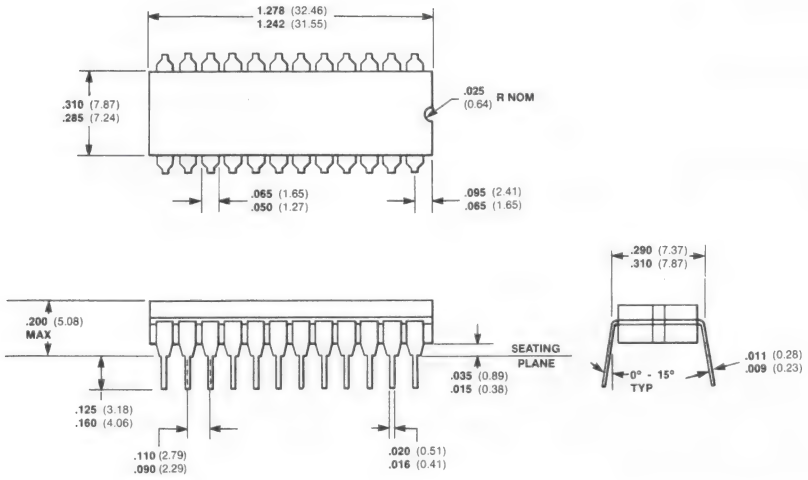
Notes
Pins are Ni/Au plated alloy 42 or equivalent
Package material is alumina, 90% min.
Lid is Ni/Au plated kovar or equivalent
Board drilling dimensions should equal your practice for **.030** (0.76) diameter holes
Pins are intended for insertion in hol rows or **.300** (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Lead angles ∝ 0° - 14°

7S 24-Pin Side-Brazed (.600)



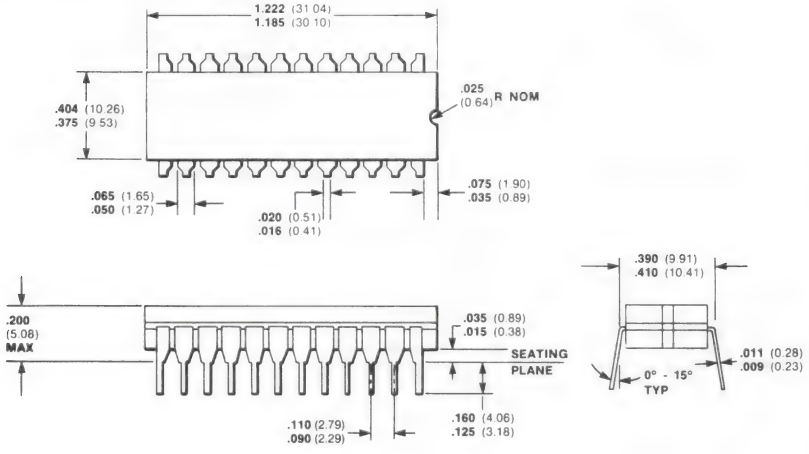
Notes
Pins are nickel/gold plated kovar or equivalent
Package material is alumina, 90% min.
Lid is Ni/Au plated kovar or equivalent
Board drilling dimensions should equal your practice for **.030** (0.76) inch diameter holes
Pins are intended for insertion hole rows on **.600** (15.24) centers
Pins are purposely shipped with "positive" misalignment to facilitate insertion
Package weight is 4 grams

4H 24-Pin Cerdip (.300)



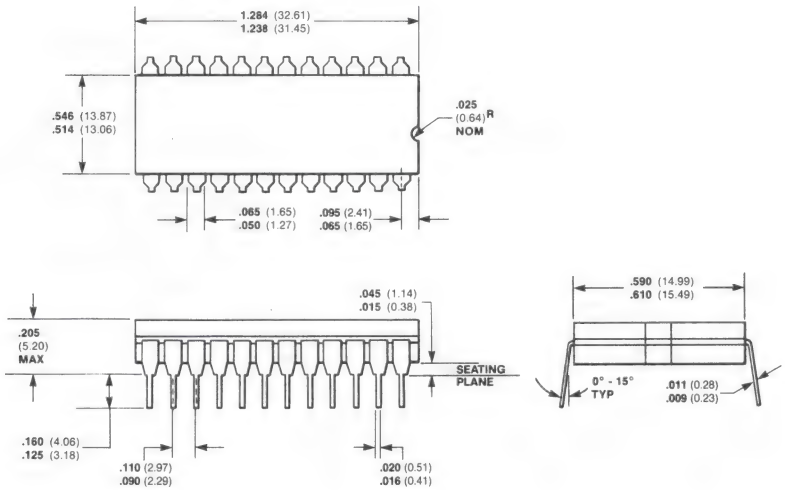
Notes
Pins are solder or tin-plated alloy 42 or equivalent
Pins are intended for insertion in hole rows on **.300** (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.030** (7.62) inch diameter pins
Hermetically sealed alumina package
Package weight is 6.7 grams
These dimensions include misalignment, glass over-run etc...
Lead thickness and width may increase by **.003** (0.08) when lead finish is applied.

6Y/SH 24-Pin Cerdip (.400)



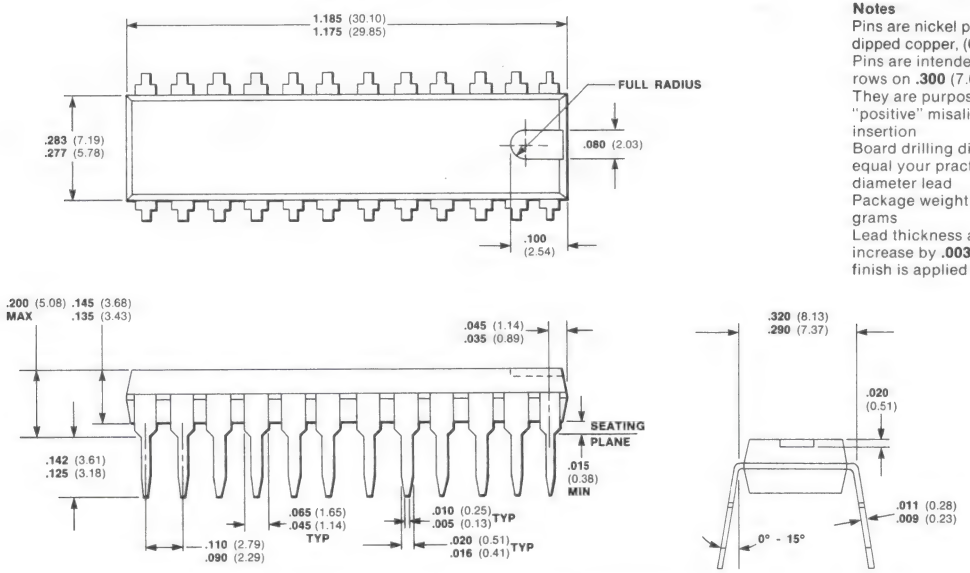
Notes
Pins are solder or tin-plated alloy 42 or equivalent
Hermetically sealed alumina package
Pins are intended for insertion in hole rows on **.400** (10.16) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Package weight is 6.0 grams
Board-drilling dimensions should equal your practice for **.030** (0.76) inch diameter holes
These dimensions include misalignment, glass over-run etc...
Lead thickness and width may increase by **.003** (0.08) when lead finish is applied

7L 24-Pin Cerdip (.600)



Notes
Pins are solder or tin-plated alloy 42 or equivalent
Hermetically sealed alumina package
Pins are intended for insertion in hole rows on **.600** (15.25) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.030** (0.76) inch diameter holes
Package weight is 7.1 grams
These dimensions include misalignment, glass over-run etc...
Lead thickness and width may increase by **.003** (0.08) when lead finish is applied.

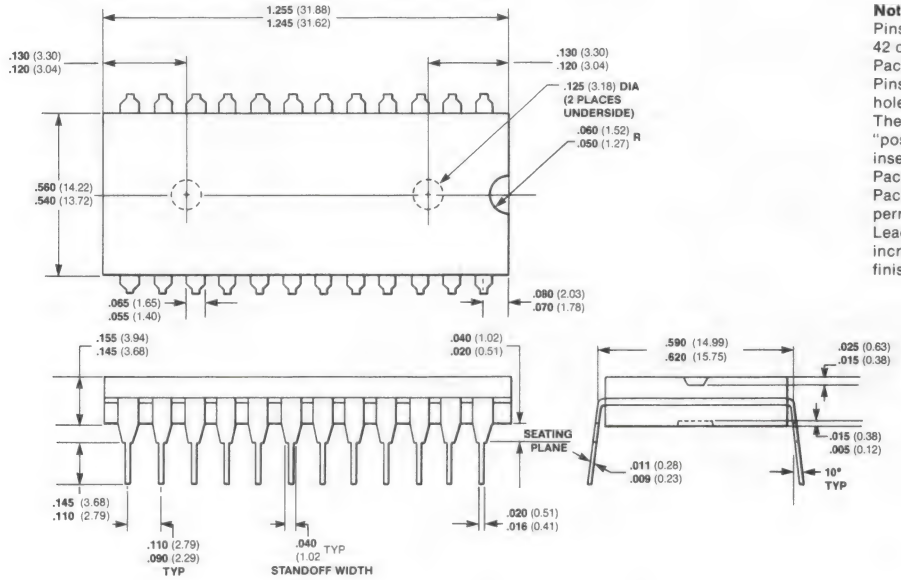
RA 24-Pin Plastic DIP (.300)



Notes
Pins are nickel plated and solder dipped copper, (Olin 195)
Pins are intended for insertion in hole rows on **.300** (7.62)
They are purposely shipped with "positive" misalignment to facilitate insertion
Board drilling dimensions should equal your practice for **.020** (0.51) diameter lead
Package weight is approximately 1.5 grams
Lead thickness and width may increase by **.003** (0.08) when lead finish is applied

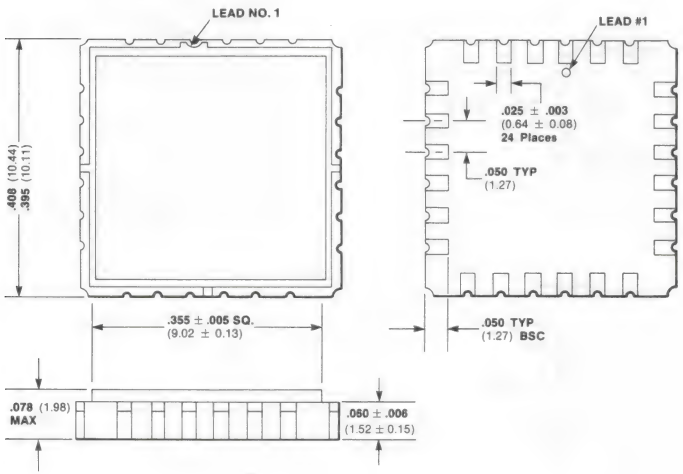
9

9N 24-Pin Plastic DIP (.600)



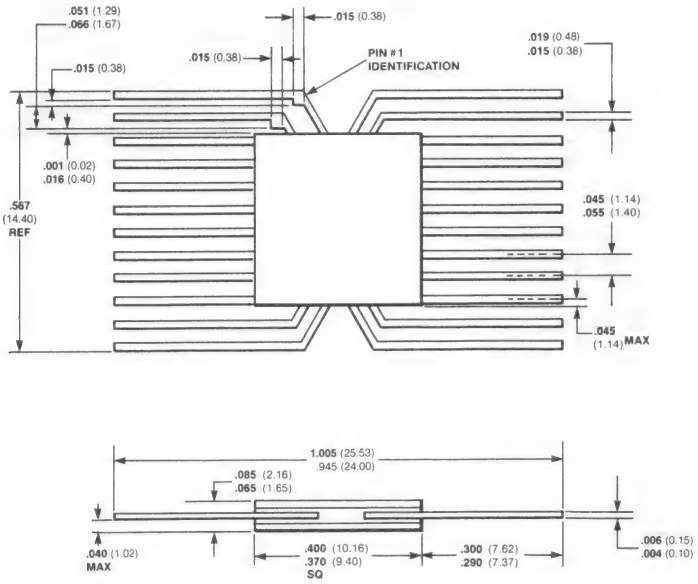
Notes
Pins are solder or tin-plated alloy 42 or equivalent
Package material is plastic
Pins are intended for insertion in hole rows on **.600** (15.24) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Package weight is 3.5 grams
Package dimensions do not include permissible flash
Lead thickness and width may increase by **.003** (0.08) when lead finish is applied

2I 24-Pin Leadless Chip Carrier



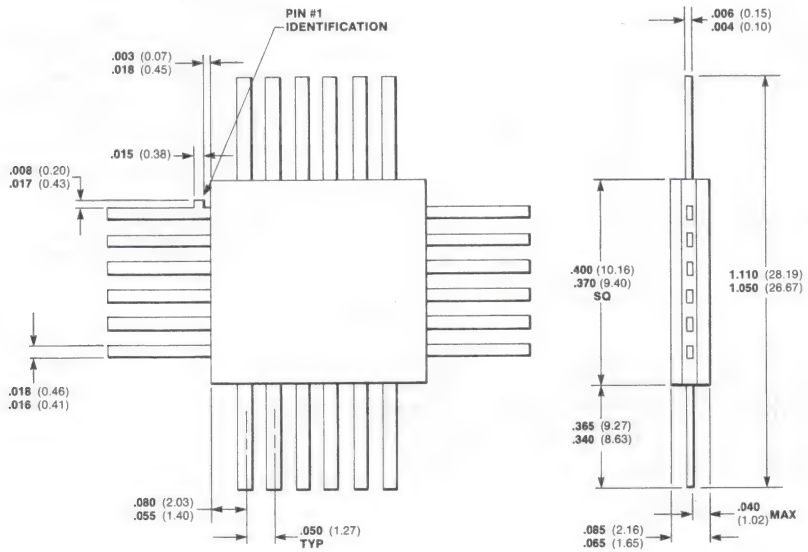
Notes
Chip carrier is 90% min. alumina, black
Cap os Ni/Au plated kovar or equivalent
All edge notches (except corners) are gold plated to connect to bottom gold lead plating
Package weight is 0.75 gram

4P 24-Pin Cerpak (.375 sq.)



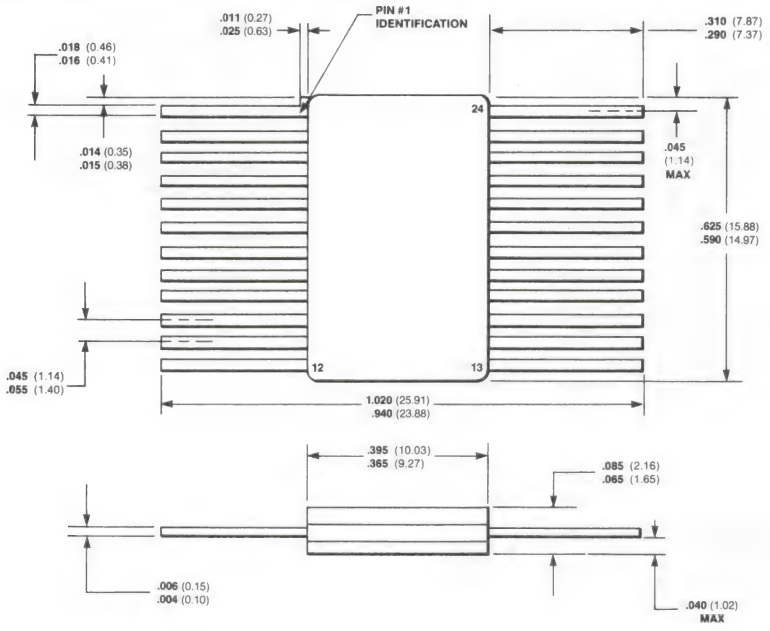
Notes
Pins are solder or tin-plated alloy 42 or equivalent
Base and cap are black alumina
Package weight is 0.8 gram
These dimensions include misalignment, glass over-run etc...
Lead thickness and width may increase by **.003** (0.08) when lead finish is applied

4V/4Q/SI 24-Pin Quad Cerpak



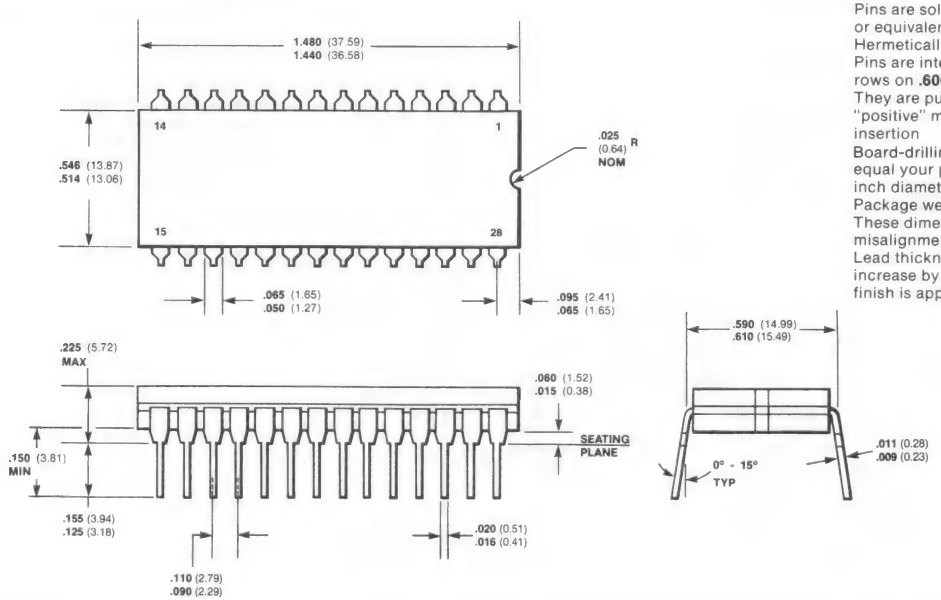
Notes
Pins are solder or tin-plated alloy 42 or equivaqlent
Package weight is 0.7 gram
These dimensions include misalignment, glass over-run etc...
Lead thickness and width may increase by **.003** (0.08) when lead finish is applied.

4X 24-Pin Cerpak (.370 x .595)



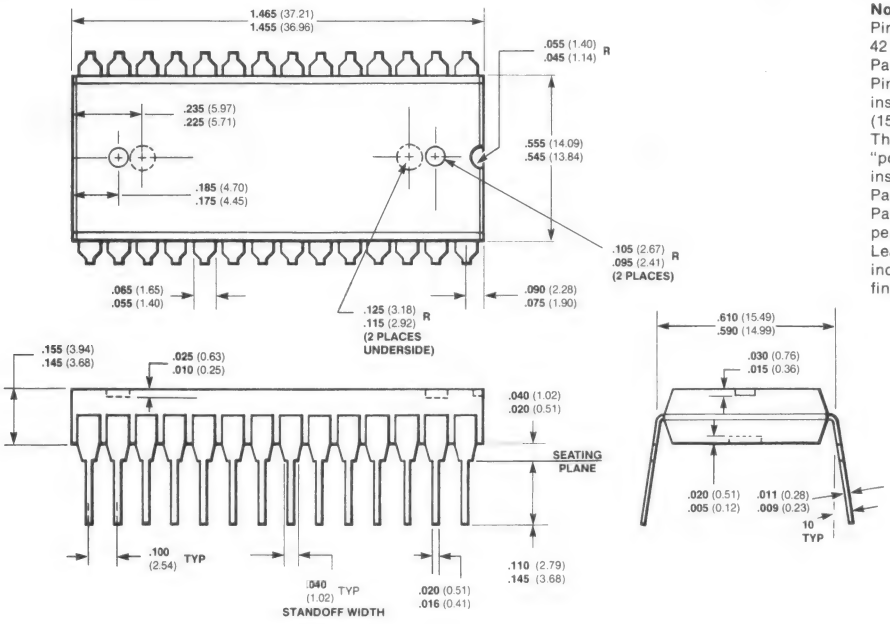
Notes
Pins are solder or tin-plated alloy 42 or equivalent
Base and cap are black alumina
Package weight is 1.0 gram
These diminsions include misalignment, glass over-run etc...
Lead thickness and width may increase by **.003** (0.08) when lead finish is applied

8S 28-Pin Cerdip (.600)



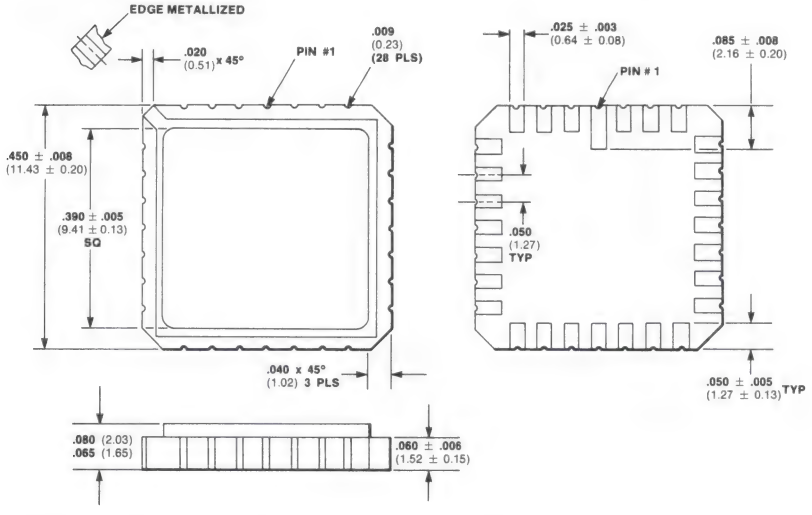
Notes
Pins are solder or tin-plated alloy 42 or equivalent
Hermetically sealed alumina package
Pins are intended for insertion in hole rows on **.600** (15.24) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.030** (0.76) inch diameter holes
Package weight is 8.6 grams
These dimensions include misalignment, glass over-run etc...
Lead thickness and width may increase by **.003** (0.08) when lead finish is applied

9Y 28-Pin Plastic DIP (.600)



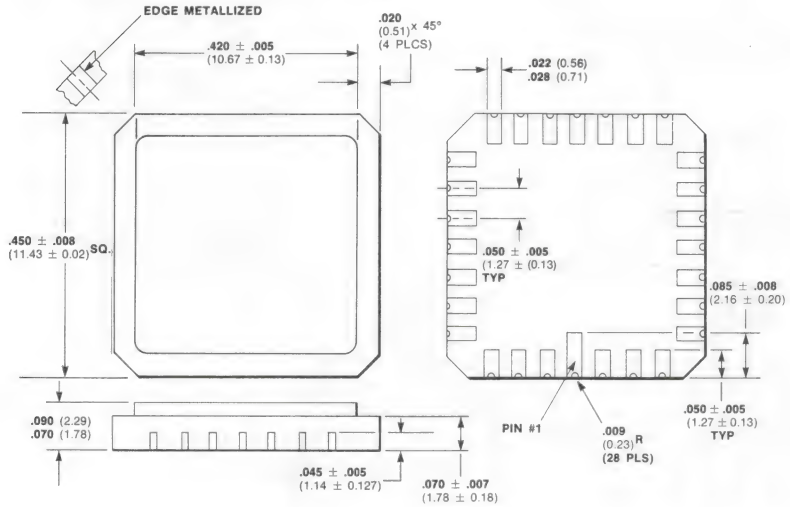
Notes
Pins are solder or tin-plated alloy 42 or equivalent
Package material is plastic
Pins are intended for intended for insertion in hole rows on **.600** (15.24) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Package weight is 4.5 grams
Package dimensions do not include permissible flash.
Lead thickness and width may increase by **.003** (0.08) when lead finish is applied.

2J 28-Pin Leadless Chip Carrier



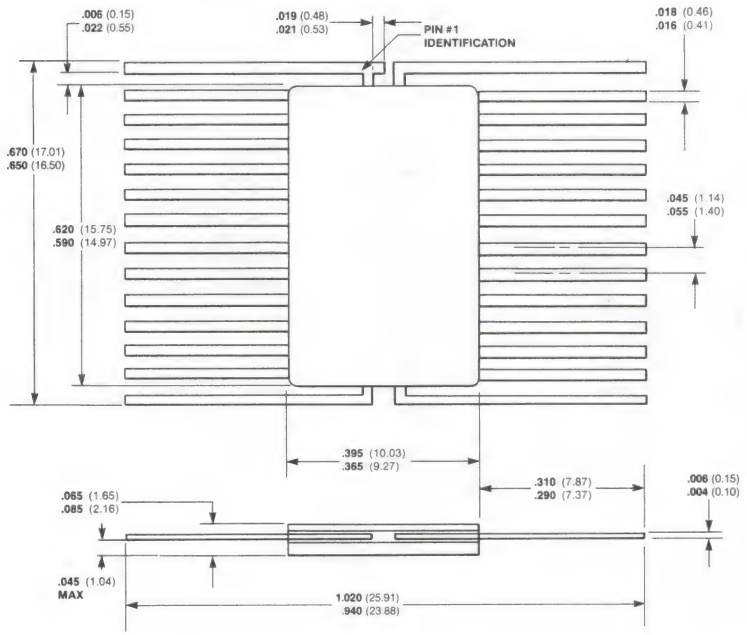
Notes
Chip carrier is 90% min. black alumina
Cap is Ni/Au plated kovar or equivalent
All edge notches (except corners) are gold plated to connect to bottom gold lead plating
Package weight is 2.7 grams

1J 28-Pin Leadless Chip Carrier



Notes
Chip carrier is 90% min. alumina, black
Cap is Ni/Au plate kovar or equivalent
All edge notches (except corners) are gold plated to connect to bottom gold lead plating
Package weight is 2.7 gram

2E 28-Pin Cerpak



Notes
Pins are solder or tin-plated alloy 42 or equivalent
Base and cap are black alumina
Package weight is 1.0 gram
These dimensions include misalignment, glass over-run etc...
Lead thickness and width increase by **.003** (0.08) when lead finish is applied

Notes

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